



# Inverter Load Rejection Over-Voltage Testing

## SolarCity CRADA Task 1a Final Report

A. Nelson, A. Hoke, and S. Chakraborty  
*National Renewable Energy Laboratory*

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*SolarCity Corporation*

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## Executive Summary

Various interconnection challenges exist when connecting distributed PV into the electrical distribution grid in terms of safety, reliability, and stability of electric power systems. One of the urgent areas for additional research - as identified by inverter manufacturers, installers, and utilities – is the potential for transient over-voltage from PV inverters. In one stage of a cooperative research and development agreement, NREL is working with SolarCity to address two specific types of transient overvoltage: load rejection overvoltage (LRO) and ground fault overvoltage (GFO). Additional partners in this effort include the Hawaiian Electric Companies, Northern Plains Power Technologies, and the Electric Power Research Institute.

This report describes testing conducted at NREL to determine the duration and magnitude of transient over-voltages created by several commercial PV inverters during load-rejection conditions. For this work, a test plan that is currently under development by the Forum on Inverter Grid Integration Issues (FIGII) has been implemented in a custom test setup at NREL. A later report describing results of GFO testing will follow.

The LRO tests were completed on a total of five commercial inverters, which included single-phase and three-phase string inverters as well as microinverters. The test inverters included a mix of single- and dual-stage topologies, as well as topologies with and without isolation transformers. The test plan included eleven different inverter power to load power settings, and all tests were repeated a total of seven times. The maximum over-voltage measured in any test did not exceed 200% of nominal, and typical over-voltage levels were significantly lower. The total voltage duration and the maximum continuous time above each threshold are presented here, as well as the time to disconnect for each test. Finally, we present a brief investigation into the effect of DC input voltage as well as a series of no-load tests.

# Contents

|  |            |
|--|------------|
| <b>Acknowledgments</b> .....                               | <b>iii</b> |
| <b>Executive Summary</b> .....                             | <b>iv</b>  |
| <b>Figures</b> .....                                       | <b>vi</b>  |
| <b>Tables</b> .....  | <b>vii</b> |
| <b>1 Introduction</b> .....                                | <b>1</b>   |
| <b>2 Test Procedures</b> .....                             | <b>2</b>   |
| 2.1 LRO Test Procedure .....                               | 2          |
| 2.2 LRO Data Reporting .....                               | 4          |
| 2.3 Test Inverters and Test Equipment Description .....    | 5          |
| <b>3 Test Results</b> .....                                | <b>6</b>   |
| 3.1 Total Time Above Voltage Thresholds .....              | 6          |
| 3.2 Maximum Continuous Time Above Voltage Thresholds ..... | 13         |
| 3.3 Maximum Instantaneous Over-voltage .....               | 18         |
| 3.4 Trip Time / Time to Disconnect .....                   | 23         |
| 3.5 Waveforms of Interest .....                            | 27         |
| Inverter 1 Waveforms .....                                 | 27         |
| Inverter 2 Waveforms .....                                 | 30         |
| Inverter 3 Waveforms .....                                 | 33         |
| Inverter 4 Waveforms .....                                 | 36         |
| Inverter 5 Waveforms .....                                 | 39         |
| 3.6 Effect of DC Input Voltage on AC Over-voltage .....    | 41         |
| 3.7 No-Load Test Results .....                             | 45         |
| <b>4 Test Procedure Recommendations</b> .....              | <b>47</b>  |
| <b>5 Conclusions and Future Work</b> .....                 | <b>47</b>  |
| <b>References</b> .....                                    | <b>48</b>  |

# Figures

|  |    |
|--|----|
| Figure 1: Generalized schematic of LRO test setup.....   | 2  |
| Figure 2: Example waveform depicting how test result data is defined .....   | 5  |
| Figure 3: Example plot of over-voltage duration as a function of voltage threshold level for a single test inverter..... | 7  |
| Figure 4: Over-voltage duration times for Inverter 1 .....   | 9  |
| Figure 5: Over-voltage duration times for Inverter 2.....  | 10 |
| Figure 6: Over-voltage duration times for Inverter 3.....  | 10 |
| Figure 7: Over-voltage duration times for Inverter 4.....  | 11 |
| Figure 8: Over-voltage duration times for Inverter 5.....  | 12 |
| Figure 9: Maximum continuous over-voltage duration times for Inverter 1 .....  | 13 |
| Figure 10: Maximum continuous over-voltage duration times for Inverter 2 .....   | 15 |
| Figure 11: Maximum continuous over-voltage duration times for Inverter 3 .....   | 16 |
| Figure 12: Maximum continuous over-voltage duration times for Inverter 4 .....   | 17 |
| Figure 13: Maximum continuous over-voltage duration times for Inverter 5 .....   | 17 |
| Figure 14: Maximum instantaneous over-voltage vs. load ratio for Inverter 1.....   | 19 |
| Figure 15: Maximum instantaneous over-voltage vs. load ratio for Inverter 2.....   | 20 |
| Figure 16: Maximum instantaneous over-voltage vs. load ratio for Inverter 3.....   | 20 |
| Figure 17: Maximum instantaneous over-voltage vs. load ratio for Inverter 4.....   | 21 |
| Figure 18: Maximum instantaneous over-voltage vs. load ratio for Inverter 5.....   | 22 |
| Figure 19: Trip time as a function of load ratio for Inverter 1.....   | 24 |
| Figure 20: Trip time as a function of load ratio for Inverter 2.....   | 25 |
| Figure 21: Trip time as a function of load ratio for Inverter 3.....   | 25 |
| Figure 22: Trip time as a function of load ratio for Inverter 4.....   | 26 |
| Figure 23: Trip time as a function of load ratio for Inverter 5.....   | 26 |
| Figure 24: Inverter 1 waveform at unity load ratio – 100% power (T11_0001).....  | 28 |
| Figure 25: Inverter 1 waveform at unity load ratio – 100% power (T11_0006).....  | 28 |
| Figure 26: Inverter 1 waveform at unity load ratio – 33% power (T33_0000).....   | 29 |
| Figure 27: Inverter 1 waveform at medium load ratio – 67% inverter / 50% load power (T56_0018) .....                     | 29 |
| Figure 28: Inverter 1 waveform at high load ratio – 100% inverter / 10% load power (T01_0000)....                        | 30 |
| Figure 29: Inverter 2 waveform at unity load ratio – 100% power (E11_0005).....  | 31 |
| Figure 30: Inverter 2 waveform at medium load ratio – 100% inverter / 67% load power (E61_0005).....                     | 31 |
| Figure 31: Inverter 2 waveform at medium/high load ratio – 67% inverter / 33% load power (E36_0000).....                 | 32 |
| Figure 32: Inverter 2 waveform at medium/high load ratio – 100% inverter / 50% load power (E51_0000).....                | 32 |
| Figure 33: Inverter 3 waveform at unity load ratio - 100% power (S11_0000).....  | 34 |
| Figure 34: Inverter 3 waveform at medium load ratio – 100% inverter / 33% load power (S31_0000).....                     | 34 |
| Figure 35: Inverter 3 waveform at high load ratio - 100% inverter / 10% load power (S01_0006)....                        | 35 |
| Figure 36: Inverter 3 waveform at high load ratio - 100% inverter / 10% load power (S01_0004)....                        | 35 |
| Figure 37: Inverter 3 waveform at unity load ratio – 33% power (S33_0002).....   | 36 |
| Figure 38: Inverter 4 waveform at unity load ratio – 100% power (P11_0000).....  | 37 |
| Figure 39: Inverter 4 waveform at unity load ratio – 100% power (P11_0001).....  | 37 |
| Figure 40: Inverter 4 waveform at medium load ratio – 100% inverter / 67% load power (P61_0001).....                     | 38 |
| Figure 41: Inverter 4 waveform at medium/high load ratio – 100% inverter / 33% load power (P31_0005).....                | 38 |
| Figure 42: Inverter 5 waveform at unity load ratio – 100% power (N11_0000).....  | 39 |
| Figure 43: Inverter 5 waveform at high load ratio – 100% inverter / 10% load power (N01_0003)....                        | 40 |
| Figure 44: Maximum AC over-voltage as a function of DC input voltage for Inverter 2.....                                 | 41 |
| Figure 45: Typical Inverter 2 response for 370 V <sub>DC</sub> input.....  | 42 |
| Figure 46: Typical Inverter 2 response for 490 V <sub>DC</sub> input.....  | 42 |

|  |    |
|--|----|
| Figure 47: Maximum AC over-voltage as a function of DC input voltage for Inverter 4 .....                        | 43 |
| Figure 48: Typical Inverter 4 response for 400 V <sub>DC</sub> input.....  | 44 |
| Figure 49: Typical Inverter 4 response for 580 V <sub>DC</sub> input.....  | 44 |
| Figure 50: Maximum over-voltage measurements for each of four test inverters at 100% output power, no load ..... | 45 |
| Figure 51: Inverter 3 waveform at 100% output power, no load.....  | 46 |

## Tables

|   |    |
|---|----|
| Table 1: EUT and resistive load power levels for each of the LRO tests .....                                    | 3  |
| Table 2: Over-voltage threshold limits.....   | 4  |
| Table 3: Basic test inverter specifications .....   | 5  |
| Table 4: Maximum (top) and average (bottom) total time above a given voltage threshold.....                     | 8  |
| Table 5: Maximum (top) and average (bottom) of the maximum continuous time above a given voltage threshold..... | 14 |
| Table 6: Maximum (top) and average (bottom) of the maximum instantaneous voltage measurement .....              | 18 |
| Table 7: Maximum (top) and average (bottom) time to disconnect for all inverters .....                          | 23 |

# 1 Introduction

The proliferation of inverter-coupled technologies such as solar photovoltaics (PV) on electric distribution systems has resulted in new opportunities to optimize distribution power systems and new challenges to prevent unstable or damaging conditions. This project addresses an urgent utility concern: the potential for transient or temporary over-voltage (TOV) from inverter-based generation such as solar PV. Transient or temporary over-voltage is of concern because of the potential to cause damage to nearby equipment and loads [1], [2]. There are two types of TOV that are of primary concern for inverter-coupled generation: load rejection over-voltage (LRO) and ground fault over-voltage (GFO) [3]. One objective of Task 1 of the NREL-SolarCity Cooperative Research and Development Agreement (CRADA) is to quantify the magnitude and duration of over-voltages caused by load rejection for inverters from different manufacturers.

This report focuses on experimental testing of LRO. GFO testing is ongoing and will be covered in a future report. LRO occurs when a portion of a distribution feeder containing a significant amount of PV and some equal or smaller amount of load becomes disconnected from the grid, resulting in a high generation to load ratio. During the brief period before higher-level inverter controls detect the disconnection of the grid, a transient overvoltage can occur when the current output from that generator is temporarily fed into the local load.

Previous authors have indicated that LRO is a concern with inverter-coupled generation [3] but have also stated that the transient over-voltage magnitude is often over-predicted, especially when inverters are viewed as simple AC current sources [2]. Hence laboratory testing is needed to determine actual LRO levels likely to be seen in the field. Some work has been done to experimentally quantify the magnitude and duration of inverter-driven LRO, but much of that work has focused on the case of an inverter being disconnected from the grid with no load or with load power exceeding generation [4]–[6]. Scenarios where no load is connected to the inverter after the grid disconnects represent the theoretical worst case in terms of over-voltage magnitude, but in such cases there is no load to be damaged by any over-voltage. Hence testing here focuses primarily on scenarios where at least some load is present.

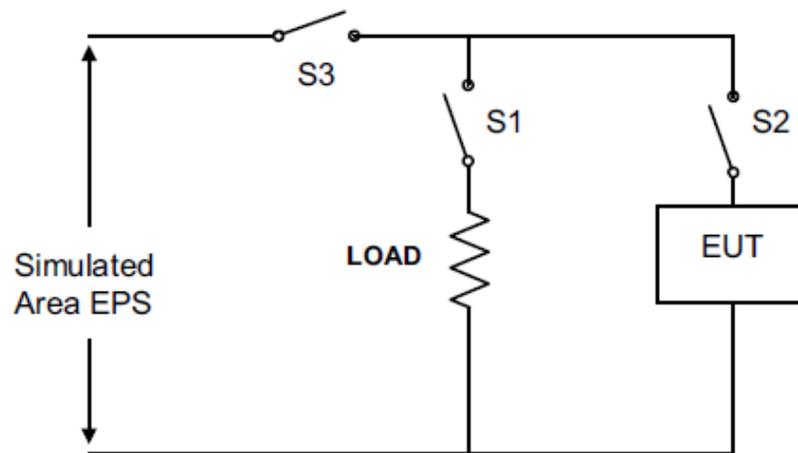
This report describes LRO testing of a broad selection of common PV inverters at a variety of generation to load ratios in accordance with a newly-developed test plan. An industry group known as the Forum on Inverter Grid Integration Issues (FIGII), which consists of members from inverter manufacturers, utilities, consultants, and research labs, developed the test plan through a consensus-based process. A total of five inverters were tested. The inverter sizes vary between 3 kW and 12 kW and both single-phase and three-phase inverters were tested individually. The testing described here serves to provide feedback to the test development process and is being used to provide input to detailed inverter model development.

## 2 Test Procedures

The test procedure used to evaluate the behavior of inverters in load-rejection scenarios is based on a draft LRO test plan written by the FIGII working group. The specific test procedures used at NREL, described below, include some minor modifications but adhere to the substantive elements of the FIGII test plan. Language that is used directly in the FIGII test procedure draft documentation has been repeated in some sections below.

### 2.1 LRO Test Procedure

The test procedure was designed to be universally applicable to all distributed resources, regardless of output power factor. However, it was written with inverter-coupled resources in mind and has not been evaluated for rotating machines (which in general may be less susceptible to LRO). Had any of the equipment under test (EUT) included controls that normally operate the unit off of unity power factor, that reactive power compensation would have remained on during the test. Also, if any of the inverters tested as part of this work had required an external or separate transformer, the transformer would have been connected between the EUT and the resistive load specified in Figure 1 and would have been considered part of the product being tested, or a mutually-coupled inductor with the equivalent impedance matching that of the specified transformer could have been connected between the EUT and the resistive load. However, none of the inverters tested during the NREL/SolarCity CRADA required external transformers or operated under non-unity power factor.



**Figure 1: Generalized schematic of LRO test setup**

For a single-phase EUT, the test circuit was configured as shown in Figure 1. The neutral connection (grounded conductor) was unaffected by the operation of switch S3. For a multiphase inverter, the balanced load circuit shown in the figure was applied between phases (delta configuration). Switch S3 was gang-operated and multi-pole. Switches S1 and S2 were for setup purposes only, and were not required for the transient part of the testing. Each EUT was connected according to the instructions and specifications provided by the manufacturer. All EUT input source parameters were set to the nominal operating conditions for the EUT, with the exception that the 300-second countdown timer to begin power export was disabled when possible in order to speed up the time between tests.

Once each EUT was ready to operate, the following sequence was executed:

1. Set the EUT (including the input source as necessary) to provide the desired output power  $\pm 2\%$ . For tests requiring less than 100% EUT nameplate output power, the maximum power limit was reduced at the EUT when the capability was available. Alternatively, input DC power to the EUT was power limited for these tests.
2. Adjust to the load resistance so that the load power is within 2% of the desired value, defined by the test scenarios in Table 1.
3. Record all applicable settings.
4. Set the Simulated EPS to the EUT nominal voltage  $\pm 2\%$  and nominal frequency  $\pm 0.1$  Hz.
5. Close switch S1, switch S2, and switch S3, and wait until the EUT produces the desired power level.
6. Open switch S3 and record the voltage versus time values across the load until the EUT ceases to energize the load. The voltage measurement was measured as close to the inverter output terminals as possible.
7. This test was performed for the combinations of EUT output and load power specified in Table 1. For all of these combinations, a value of 100% was taken to mean 100% of the EUT's nameplate rating. The "Yes" or "No" entries indicate whether that test was performed.
8. The tests for each output/load combination were repeated for a total of seven (7) samples each, ensuring that switch S3 was opened at different portions on the line cycle.

**Table 1: EUT and resistive load power levels for each of the LRO tests**

| Load power (% of EUT rated power) ►<br>EUT output ▼ | 100% | 66% | 50% | 33% | 10% |
|---|------|-----|-----|-----|-----|
| 100%  | Yes  | Yes | Yes | Yes | Yes |
| 66%   | No   | Yes | Yes | Yes | Yes |
| 33%   | No   | No  | No  | Yes | Yes |

Since the EUTs required a separate test input source to conduct this test, that source was capable of supplying at least 150% of the maximum input power rating of the EUT over the entire range of EUT input voltages.

The test and measurement equipment recorded each phase current and each phase-to-neutral voltage (for three-phase tests) or line-to-line voltage (for single-phase tests) over the duration of the test. A sampling frequency of at least 15 kHz was required for load voltage and current measurements; the actual sampling frequency during these tests was 50 kHz.

An area EPS source means any source capable of emulating a utility source by acting as a constant AC voltage source, maintaining the voltage and frequency within the recommended

windows. Tests at NREL were conducted using a unidirectional power electronic AC voltage source. Because the power supply cannot sink power, an additional shunt resistive load bank was connected between the AC source and switch S3 to absorb the excess EUT power. Because this load bank is on the EPS side of switch S3, it is disconnected from the EUT when the load rejection occurs and does not affect the results of the test.

## 2.2 LRO Data Reporting

A voltage-duration curve was created using sampled instantaneous voltage measurements during the complete transient time of the inverter. The number of voltage measurements above the voltage levels provided in Table 2 was multiplied by the sample interval, resulting in that voltage threshold's total duration. Note that at the end of this report we include a recommendation to modify the voltage levels shown in Table 2. The voltage-duration curve is a plot of all points (voltage, duration) derived from this process.

**Table 2: Over-voltage threshold limits**

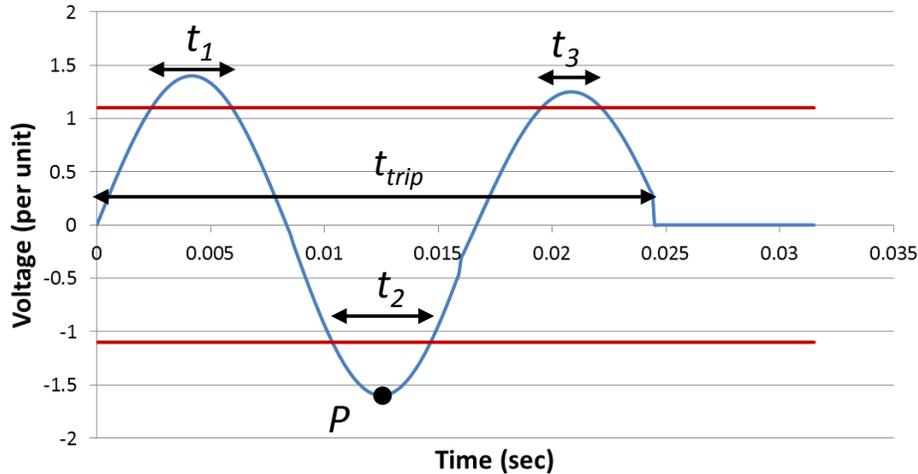
| Instantaneous Voltage (% of nominal peak voltage) |
|---|
| 500   |
| 200   |
| 140   |
| 120   |
| 110   |

The voltage levels shown in Table 2 were originally derived from voltage levels in what is known as the CBEMA<sup>1</sup> curve, or its successor the ITIC<sup>2</sup> curve, both of which describe the tolerance of electronic equipment to voltage surges of varying durations. However, FIGII working group members generally agreed that these curves may not actually be appropriate for evaluating inverter behavior in load rejection scenarios because they were not designed for that purpose, and because utilities may not hold even their own distribution equipment and surge arrestors to such a stringent standard. In the conclusion of this report we suggest modifying the voltage levels in Table 2 to better capture observed load rejection behavior.

In addition, the longest time that the voltage exceeded each of the limits in Table 2 *continuously* was recorded for each of the test settings. The distinction between the total voltage duration time and the maximum continuous time is depicted in Figure 2. For waveforms that exceed a defined voltage threshold during multiple parts of the cycle (either positive or negative polarity), the total voltage duration will always be greater than the maximum continuous time. For the example waveform given, the total voltage duration would be recorded as the sum of  $t_1$ ,  $t_2$ , and  $t_3$ . Since  $t_2$  is the longest continuous time the voltage exceeds the threshold,  $t_2$  would be recorded for the longest continuous duration metric.

<sup>1</sup> Computer Business Equipment Manufacturers Association

<sup>2</sup> Information Technology Industry Council



**Figure 2: Example waveform depicting how test result data is defined**

In addition to the voltage duration metrics described, the absolute value of the maximum instantaneous voltage measurement recorded at any time during the transient event is reported (as represented by the voltage at point P in Figure 2), as well as the trip time (represented by  $t_{trip}$ ). For the purposes of these tests, the trip time was defined as the time between switch S3 opening and the EUT mains voltage dropping below a threshold and never again exceeding that threshold.

### 2.3 Test Inverters and Test Equipment Description

The basic specifications for the test inverters are given in Table 3. For the purposes of this report, the inverter manufacturer and model number are not given, and inverters are given a generic name (“Inverter 1”, Inverter 2”, ...). As seen in the table, a variety of inverter topologies and power levels have been selected for this study.

**Table 3: Basic test inverter specifications**

|            | <b>Voltage Configuration</b> | <b>Nameplate Power</b> | <b>Additional Information</b>                           |
|------------|------------------------------|------------------------|---|
| Inverter 1 | 240 V Split Phase            | 6.0 kW                 | Dual stage, transformerless                             |
| Inverter 2 | 240 V Split Phase            | 6.0 kW                 | Single stage, transformerless                           |
| Inverter 3 | 240 V Split Phase            | 3.0 kW                 | Single stage, internal 60 Hz transformer                |
| Inverter 4 | 480 V Three Phase            | 12.0 kW                | Dual stage, transformerless                             |
| Inverter 5 | 208 V Three Phase            | 4.5 kW                 | 18x 250 W microinverters in a three-phase configuration |

The major test and measurement equipment used in this testing were as follows:

- Grid Simulator: Pacific Power 3060-MS/3235 62.5 kVA AC power supply with isolation transformer and UPC32 programmable controller
- DC Input Source (central/string inverters): AV-900 300 A, 900 V, 250 kW dual channel DC power supply
- DC Input Source (microinverters): TerraSAS PV supply, 14x ETS60X14C-PVF and 4x ETS80X10.5C-PVF modules
- Resistive Load Banks: Simplex Neptune 100 kW, 173 kVAR RL load bank and Simplex Titan 436 kVA at  $\pm 0.37$  power factor RLC load bank
- Yokogawa DL850E Scopercorder, calibration date 08/2014, 720210/701250 modules for power measurements, 701267 modules for signal measurements
- Yokogawa 700924 differential voltage probes (1:100 setting)
- Yokogawa 701930/701931 current probes (10 mV/A, 150/500 A maximum)
- AEMC MR 561 current probe (10 mV/A, 150 A maximum)
- AEMC MN 261 current probe (10 mV/A, 200 A maximum)
- Fluke 87 RMS multimeter

### 3 Test Results

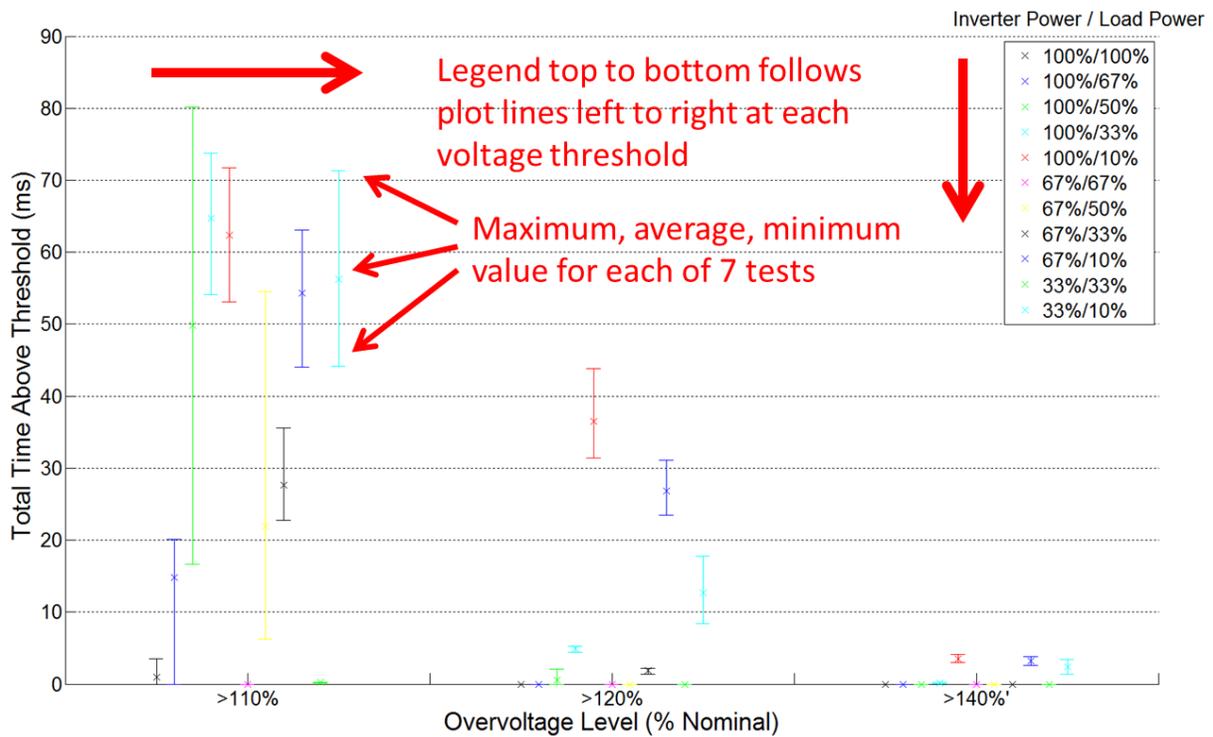
All test results for LRO testing are provided in the following sections for each of the five test inverters. Each section contains mean values and maximum/minimum values for each of the inverter/load power test settings, across a total of seven tests at each setting. The first sections contain data about total over-voltage durations, maximum continuous over-voltage durations, maximum voltage measurements, and trip times. Representative waveforms and waveforms of particular interest are provided in the subsequent section for each test inverter. Finally, an exploration of the effect of DC input voltage for two of the test inverters is provided, followed by a discussion of no-load test results.

#### 3.1 Total Time Above Voltage Thresholds

The total over-voltage duration curves for each of the five test inverters are provided below. These plots display the total amount of time that the voltage at the AC terminals exceeded each of the voltage thresholds given in Table 2. Each measurement is inclusive of higher threshold limits; for example, time above the 120% threshold includes time above the 140%, 200%, and 500% thresholds. For three-phase inverters (Inverter 4 and Inverter 5), these plots show the total time that any of the three phases exceeded a given threshold (the sum of the three phases).

An example over-voltage duration plot is shown in Figure 3. The legend shows each of the 11 inverter power and load power test settings, and a plot is given at each of these test settings for each voltage threshold. The legend reads top to bottom as the plot points read left to right for each voltage threshold level. Each whisker plot shows the average (mean) value of the seven test runs, along with the maximum and minimum values of these tests. The overall test data are

summarized in Table 4, which contains all of the information about averages and maxima that is contained in individual inverter plots. All time measurements are reported in milliseconds (ms), and only the 110%/120%/140% voltage thresholds are reported because no instantaneous voltage measurement exceeded the 200% voltage threshold.



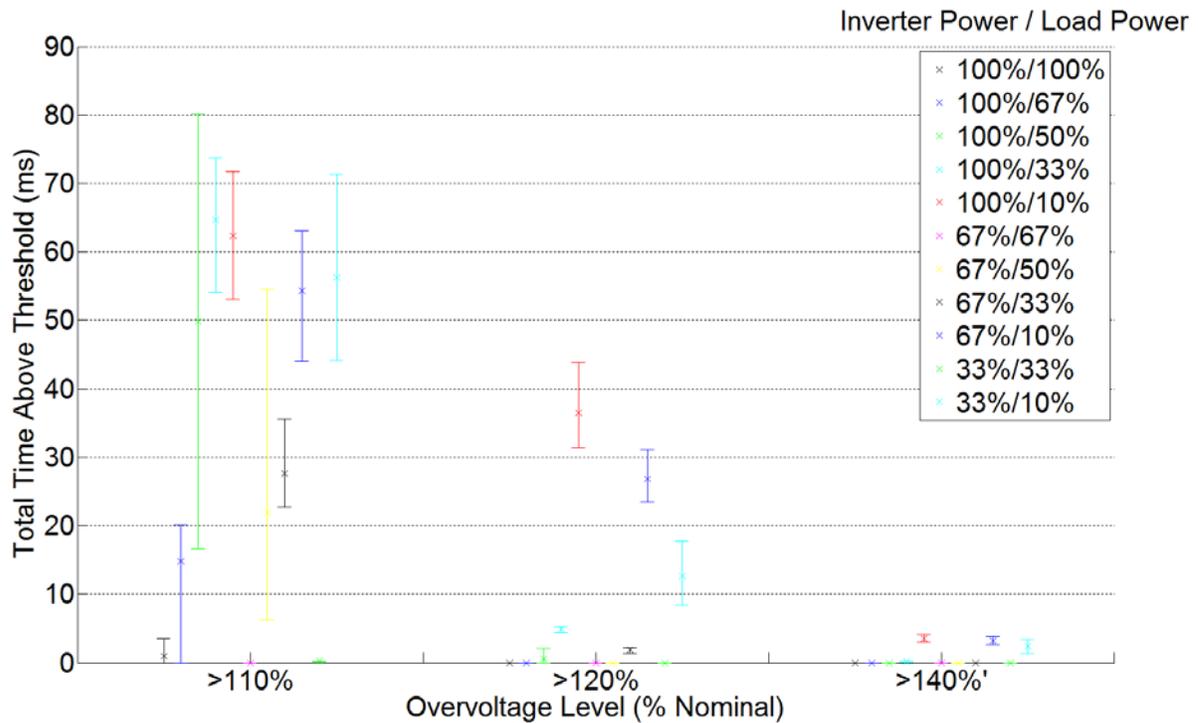
**Figure 3: Example plot of over-voltage duration as a function of voltage threshold level for a single test inverter**

| Test Setting       |                | Maximum Total Time Above a Given Over-voltage Threshold (ms) |      |      |            |      |      |            |      |      |            |      |      |            |      |      |
|--------------------|----------------|--|------|------|------------|------|------|------------|------|------|------------|------|------|------------|------|------|
|                    |                | Inverter 1   |      |      | Inverter 2 |      |      | Inverter 3 |      |      | Inverter 4 |      |      | Inverter 5 |      |      |
| Inverter Power (%) | Load Power (%) | 110%   | 120% | 140% | 110%       | 120% | 140% | 110%       | 120% | 140% | 110%       | 120% | 140% | 110%       | 120% | 140% |
| 100                | 100            | 3.5  | 0.0  | 0.0  | 0.0        | 0.0  | 0.0  | 2.1        | 0.0  | 0.0  | 23.3       | 10.4 | 0.7  | 0.0        | 0.0  | 0.0  |
| 100                | 67             | 20.1   | 0.0  | 0.0  | 57.6       | 0.0  | 0.0  | 4.7        | 4.1  | 1.3  | 6.5        | 1.4  | 0.0  | 10.2       | 8.4  | 1.9  |
| 100                | 50             | 80.2   | 2.1  | 0.0  | 102.3      | 0.4  | 0.0  | 1.7        | 1.4  | 0.9  | 6.8        | 2.1  | 0.0  | 5.3        | 4.3  | 1.7  |
| 100                | 33             | 73.8   | 5.3  | 0.2  | 102.6      | 0.7  | 0.0  | 3.0        | 2.9  | 1.5  | 8.7        | 2.4  | 0.0  | 7.4        | 5.3  | 1.1  |
| 100                | 10             | 71.7   | 43.8 | 4.1  | 80.5       | 3.6  | 0.1  | 4.7        | 4.2  | 1.0  | 8.2        | 1.6  | 0.0  | 6.7        | 5.0  | 2.1  |
| 67                 | 67             | 0.0  | 0.0  | 0.0  | 0.0        | 0.0  | 0.0  | 0.0        | 0.0  | 0.0  | 4.6        | 1.7  | 0.0  | 0.0        | 0.0  | 0.0  |
| 67                 | 50             | 54.6   | 0.0  | 0.0  | 71.9       | 0.0  | 0.0  | 14.0       | 7.1  | 0.0  | 8.6        | 2.0  | 0.0  | 5.8        | 4.2  | 0.7  |
| 67                 | 33             | 35.6   | 2.2  | 0.0  | 118.3      | 0.4  | 0.0  | 4.1        | 3.4  | 0.6  | 8.5        | 4.0  | 0.0  | 6.3        | 5.2  | 2.1  |
| 67                 | 10             | 63.1   | 31.1 | 3.8  | 84.7       | 2.4  | 0.0  | 6.0        | 4.8  | 1.6  | 4.9        | 0.5  | 0.0  | 10.9       | 8.7  | 2.1  |
| 33                 | 33             | 0.3  | 0.0  | 0.0  | 0.9        | 0.0  | 0.0  | 46.1       | 28.5 | 1.5  | 2.2        | 0.6  | 0.0  | 0.0        | 0.0  | 0.0  |
| 33                 | 10             | 71.3   | 17.7 | 3.5  | 72.5       | 0.5  | 0.0  | 7.7        | 6.6  | 1.8  | 4.3        | 0.6  | 0.0  | 4.3        | 3.5  | 1.3  |

| Test Setting       |                | Average Total Time Above a Given Over-voltage Threshold (ms) |      |      |            |      |      |            |      |      |            |      |      |            |      |      |
|--------------------|----------------|--|------|------|------------|------|------|------------|------|------|------------|------|------|------------|------|------|
|                    |                | Inverter 1   |      |      | Inverter 2 |      |      | Inverter 3 |      |      | Inverter 4 |      |      | Inverter 5 |      |      |
| Inverter Power (%) | Load Power (%) | 110%   | 120% | 140% | 110%       | 120% | 140% | 110%       | 120% | 140% | 110%       | 120% | 140% | 110%       | 120% | 140% |
| 100                | 100            | 0.9  | 0.0  | 0.0  | 0.0        | 0.0  | 0.0  | 1.2        | 0.0  | 0.0  | 7.2        | 3.1  | 0.1  | 0.0        | 0.0  | 0.0  |
| 100                | 67             | 14.8   | 0.0  | 0.0  | 55.6       | 0.0  | 0.0  | 2.6        | 2.1  | 0.8  | 2.5        | 0.3  | 0.0  | 4.5        | 3.3  | 0.7  |
| 100                | 50             | 49.8   | 0.6  | 0.0  | 92.7       | 0.1  | 0.0  | 1.6        | 1.3  | 0.8  | 4.1        | 0.9  | 0.0  | 2.8        | 2.0  | 0.7  |
| 100                | 33             | 64.7   | 4.9  | 0.2  | 66.4       | 0.5  | 0.0  | 1.7        | 1.5  | 0.9  | 4.6        | 0.8  | 0.0  | 4.5        | 2.9  | 0.5  |
| 100                | 10             | 62.4   | 36.5 | 3.5  | 70.1       | 2.8  | 0.0  | 2.5        | 2.1  | 0.8  | 3.9        | 0.7  | 0.0  | 4.9        | 3.6  | 1.5  |
| 67                 | 67             | 0.0  | 0.0  | 0.0  | 0.0        | 0.0  | 0.0  | 0.0        | 0.0  | 0.0  | 2.7        | 1.0  | 0.0  | 0.0        | 0.0  | 0.0  |
| 67                 | 50             | 21.9   | 0.0  | 0.0  | 71.1       | 0.0  | 0.0  | 8.2        | 4.9  | 0.0  | 4.0        | 0.8  | 0.0  | 4.3        | 3.0  | 0.1  |
| 67                 | 33             | 27.7   | 1.8  | 0.0  | 91.4       | 0.2  | 0.0  | 2.5        | 1.8  | 0.2  | 3.0        | 0.9  | 0.0  | 3.0        | 2.4  | 0.8  |
| 67                 | 10             | 54.3   | 26.9 | 3.2  | 64.2       | 1.5  | 0.0  | 3.0        | 2.3  | 0.9  | 2.4        | 0.3  | 0.0  | 5.1        | 3.5  | 1.0  |
| 33                 | 33             | 0.3  | 0.0  | 0.0  | 0.1        | 0.0  | 0.0  | 11.7       | 7.5  | 0.2  | 0.5        | 0.1  | 0.0  | 0.0        | 0.0  | 0.0  |
| 33                 | 10             | 56.3   | 12.7 | 2.3  | 63.1       | 0.3  | 0.0  | 4.5        | 3.7  | 0.3  | 2.4        | 0.2  | 0.0  | 1.9        | 1.5  | 0.6  |

**Table 4: Maximum (top) and average (bottom) total time above a given voltage threshold**

A plot of the voltage duration ranges for Inverter 1 is shown in Figure 4. The largest measured over-voltage duration above 110% of nominal was 80.2 ms and the largest duration above 120% of nominal was 43.8 ms. Over-voltage duration times tended to increase with increasing load ratios (inverter power divided by load power), and this inverter had few over-voltage measurements above the 140% threshold.



**Figure 4: Over-voltage duration times for Inverter 1**

A plot of the voltage duration ranges for Inverter 2 is shown in Figure 5. The largest measured over-voltage duration above 110% of nominal was 118.3 ms. This inverter tended to have the longest over-voltage duration times above the 110% threshold, but spent little or no time above the 120% and 140% thresholds. Over-voltage duration times tended to increase with increasing load ratios, and almost no over-voltage measurements were recorded for unity load ratios.

A plot of the voltage duration ranges for Inverter 3 is shown in Figure 6. The largest measured over-voltage duration above 110% of nominal was 46.1 ms, which occurred during one test at the 33%/33% inverter/load power setting. Other than this single outlier, all over-voltage duration times were less than a single 60 Hz AC cycle, with significantly shorter over-voltage duration times than the other single phase inverters (Inverter 1 and Inverter 2). The output waveform of the single outlier test is presented later in this report.

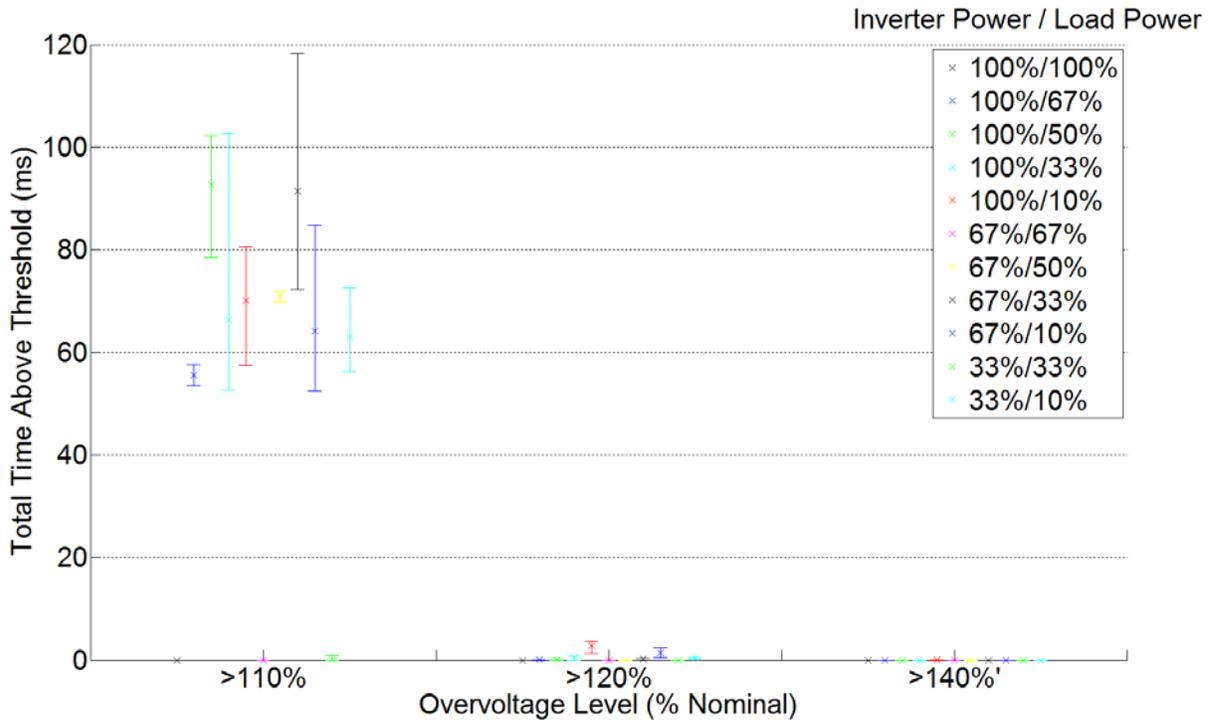


Figure 5: Over-voltage duration times for Inverter 2

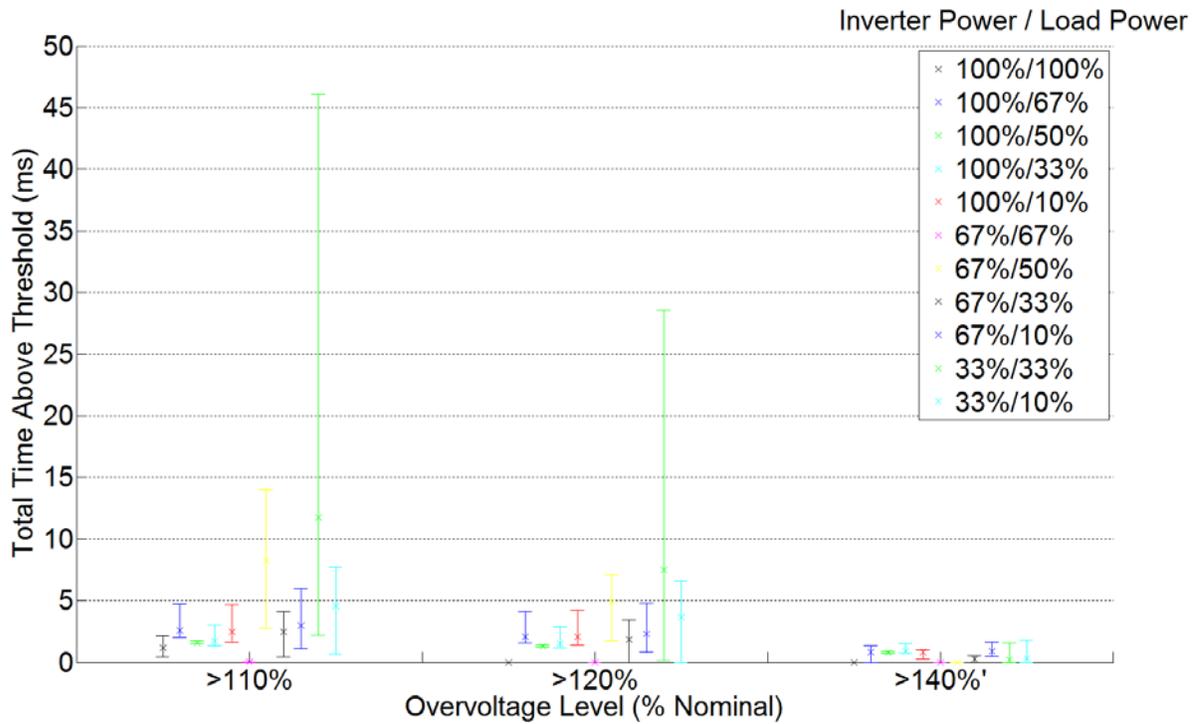
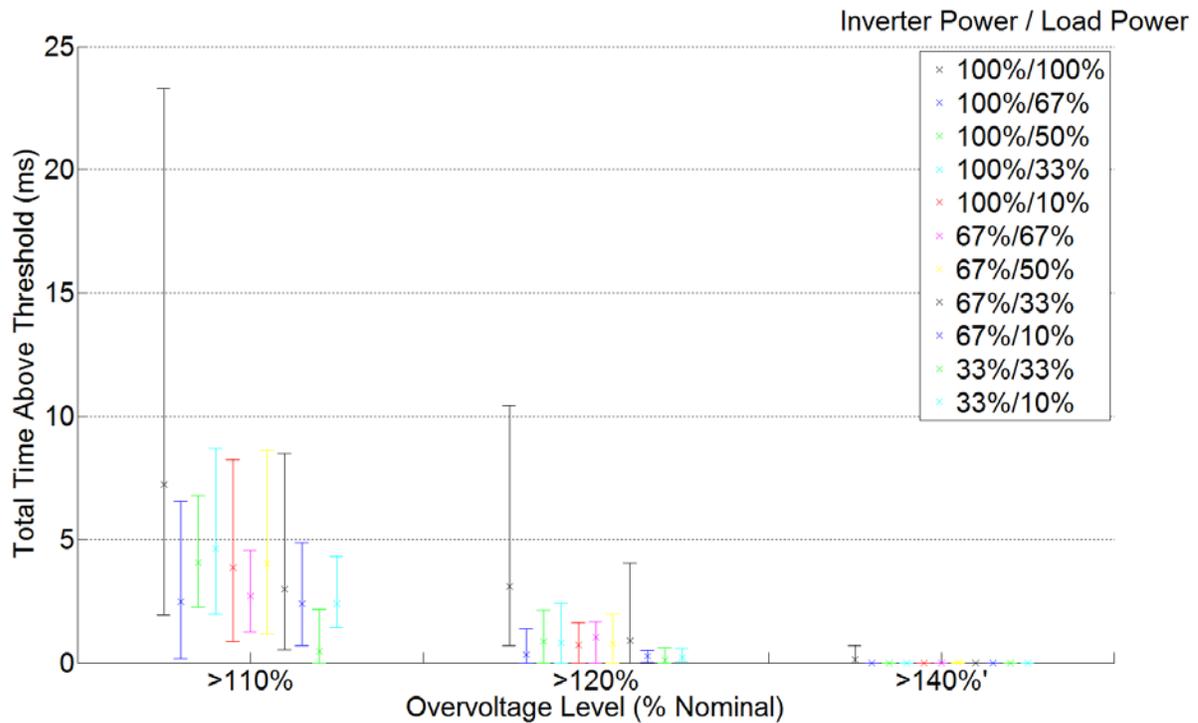


Figure 6: Over-voltage duration times for Inverter 3

A plot of the voltage duration ranges for Inverter 4 is shown in Figure 7. The largest measured over-voltage duration above 110% of nominal was 23.3 ms. Similar to Inverter 3, this largest over-voltage duration was recorded during a single test that is displayed later in this report. No other over-voltage time exceeded a single AC cycle, and very few measurements above the 140% threshold were recorded.



**Figure 7: Over-voltage duration times for Inverter 4**

A plot of the voltage duration ranges for Inverter 5 is shown in Figure 8. The largest measured over-voltage duration above 110% of nominal was 10.9 ms. This inverter had consistently short over-voltage duration times, and no over-voltage measurements above 110% of nominal were recorded for unity load ratio tests.

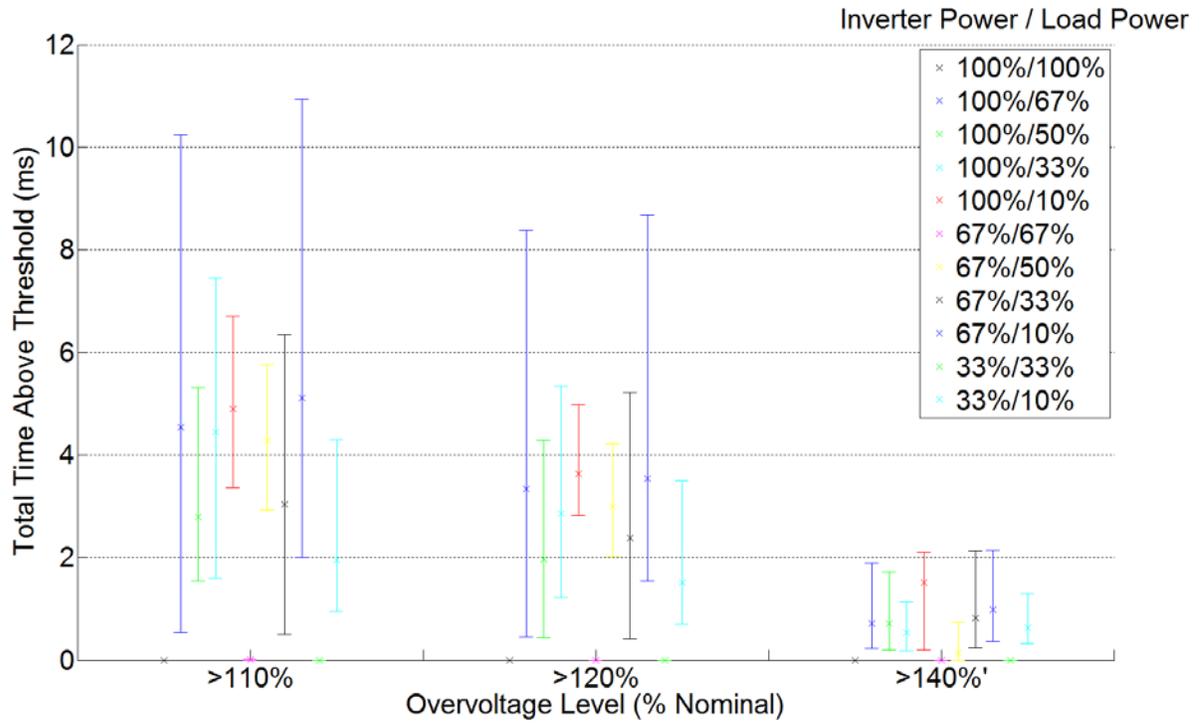


Figure 8: Over-voltage duration times for Inverter 5

### 3.2 Maximum Continuous Time Above Voltage Thresholds

A summary of the maximums and averages of the maximum continuous time spent above each voltage threshold is shown in Table 5. Since no instantaneous voltage measurement exceeded 200% of nominal in any test, only the 110%/120%/140% thresholds are reported in this table. As described earlier, the maximum continuous time variables by definition are less than or equal to the total time durations reported in the previous section. Averages and maximums are calculated from a set of seven tests executed at each loading ratio. For three-phase inverters, this data set shows the maximum continuous time that any individual phase voltage exceeded a given threshold. It is possible that the maximum continuous over-voltage occurred on different phases for different voltage thresholds.

A plot of the maximum continuous over-voltage duration ranges for Inverter 1 is shown in Figure 9. The largest measured continuous over-voltage duration above 110% of nominal was 7.38 ms. Over-voltage durations tended to increase with increasing load ratio, and very little time was spent above the 120% and 140% thresholds.

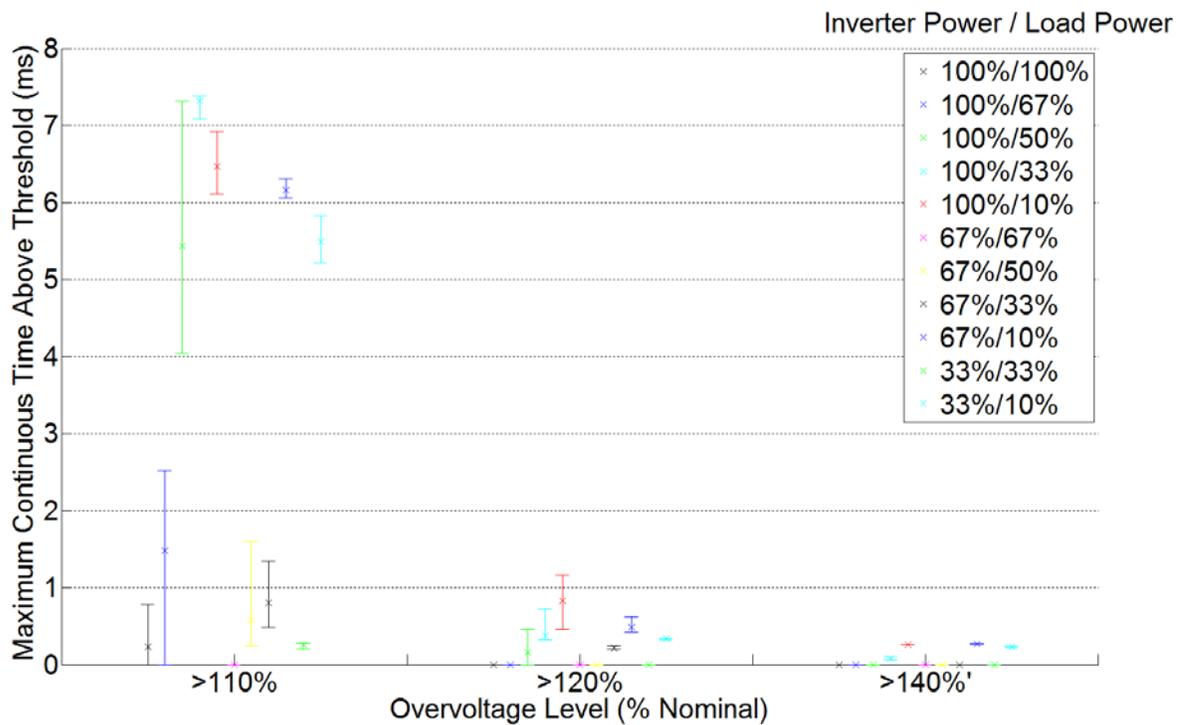


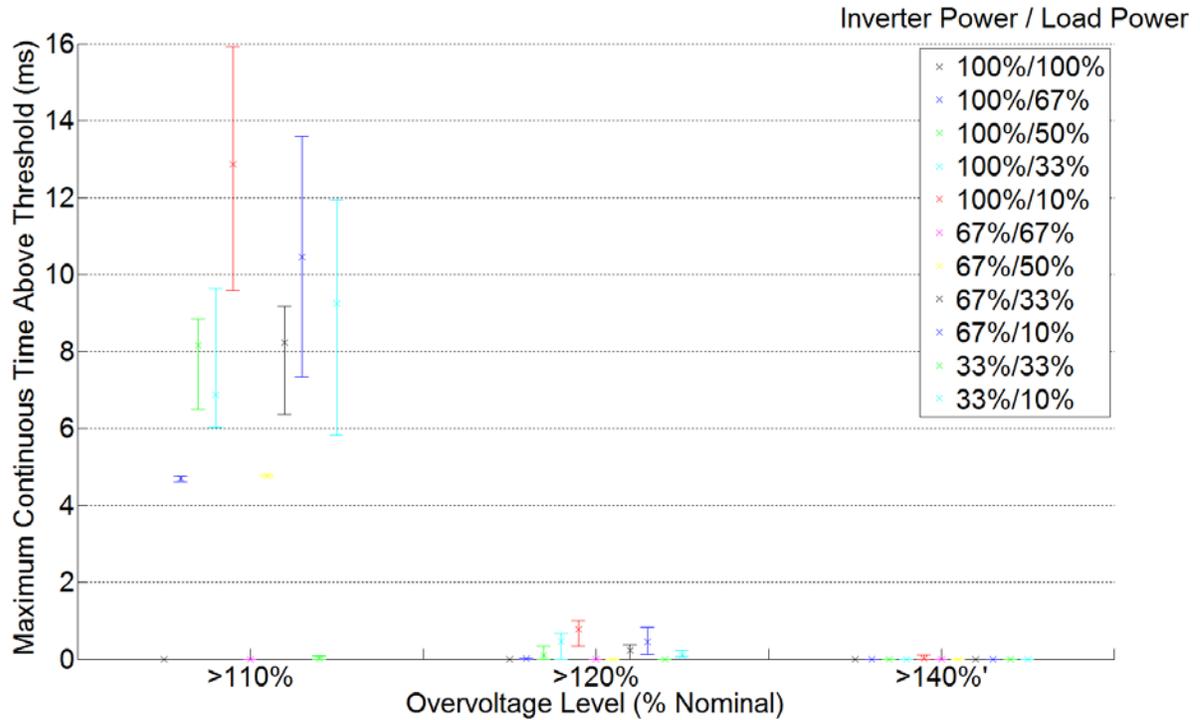
Figure 9: Maximum continuous over-voltage duration times for Inverter 1

| Test Setting       |                | Maximum Continuous Time Above a Given Over-voltage Threshold (ms) |      |      |            |      |      |            |      |      |            |      |      |            |      |      |
|--------------------|----------------|---|------|------|------------|------|------|------------|------|------|------------|------|------|------------|------|------|
|                    |                | Inverter 1  |      |      | Inverter 2 |      |      | Inverter 3 |      |      | Inverter 4 |      |      | Inverter 5 |      |      |
| Inverter Power (%) | Load Power (%) | 110%  | 120% | 140% | 110%       | 120% | 140% | 110%       | 120% | 140% | 110%       | 120% | 140% | 110%       | 120% | 140% |
| 100                | 100            | 0.78  | 0.00 | 0.00 | 0.00       | 0.00 | 0.00 | 0.76       | 0.00 | 0.00 | 2.92       | 2.22 | 0.50 | 0.00       | 0.00 | 0.00 |
| 100                | 67             | 2.52  | 0.00 | 0.00 | 4.76       | 0.02 | 0.00 | 3.38       | 2.92 | 0.92 | 2.30       | 0.64 | 0.00 | 3.72       | 2.96 | 0.84 |
| 100                | 50             | 7.32  | 0.46 | 0.00 | 8.84       | 0.34 | 0.00 | 1.54       | 1.38 | 0.90 | 2.38       | 1.48 | 0.00 | 4.46       | 3.74 | 1.72 |
| 100                | 33             | 7.38  | 0.72 | 0.10 | 9.64       | 0.66 | 0.00 | 3.00       | 2.86 | 1.48 | 4.14       | 1.68 | 0.00 | 3.50       | 2.76 | 1.06 |
| 100                | 10             | 6.92  | 1.16 | 0.26 | 15.92      | 1.00 | 0.10 | 2.90       | 2.76 | 1.00 | 4.40       | 0.80 | 0.00 | 3.44       | 2.74 | 2.06 |
| 67                 | 67             | 0.00  | 0.00 | 0.00 | 0.00       | 0.00 | 0.00 | 0.02       | 0.00 | 0.00 | 2.16       | 1.66 | 0.00 | 0.02       | 0.00 | 0.00 |
| 67                 | 50             | 1.60  | 0.00 | 0.00 | 4.80       | 0.00 | 0.00 | 3.80       | 3.08 | 0.00 | 4.60       | 0.84 | 0.02 | 3.62       | 2.94 | 0.12 |
| 67                 | 33             | 1.34  | 0.24 | 0.00 | 9.16       | 0.38 | 0.00 | 1.72       | 1.48 | 0.46 | 4.20       | 1.56 | 0.00 | 4.74       | 4.30 | 1.82 |
| 67                 | 10             | 6.30  | 0.62 | 0.28 | 13.58      | 0.82 | 0.00 | 2.36       | 2.00 | 0.90 | 1.54       | 0.26 | 0.00 | 5.38       | 4.52 | 1.38 |
| 33                 | 33             | 0.28  | 0.00 | 0.00 | 0.08       | 0.00 | 0.00 | 4.64       | 3.86 | 0.54 | 1.70       | 0.30 | 0.00 | 0.00       | 0.00 | 0.00 |
| 33                 | 10             | 5.82  | 0.34 | 0.24 | 11.94      | 0.22 | 0.00 | 3.96       | 3.70 | 0.60 | 1.50       | 0.28 | 0.00 | 2.74       | 2.30 | 0.74 |

| Test Setting       |                | Average Maximum Continuous Time Above a Given Over-voltage Threshold (ms) |      |      |            |      |      |            |      |      |            |      |      |            |      |      |
|--------------------|----------------|---|------|------|------------|------|------|------------|------|------|------------|------|------|------------|------|------|
|                    |                | Inverter 1  |      |      | Inverter 2 |      |      | Inverter 3 |      |      | Inverter 4 |      |      | Inverter 5 |      |      |
| Inverter Power (%) | Load Power (%) | 110%  | 120% | 140% | 110%       | 120% | 140% | 110%       | 120% | 140% | 110%       | 120% | 140% | 110%       | 120% | 140% |
| 100                | 100            | 0.23  | 0.00 | 0.00 | 0.00       | 0.00 | 0.00 | 0.36       | 0.00 | 0.00 | 1.96       | 1.05 | 0.11 | 0.00       | 0.00 | 0.00 |
| 100                | 67             | 1.48  | 0.00 | 0.00 | 4.69       | 0.00 | 0.00 | 2.24       | 1.89 | 0.69 | 1.15       | 0.22 | 0.00 | 2.17       | 1.44 | 0.39 |
| 100                | 50             | 5.43  | 0.16 | 0.00 | 8.16       | 0.10 | 0.00 | 1.49       | 1.29 | 0.78 | 1.72       | 0.42 | 0.00 | 1.97       | 1.47 | 0.58 |
| 100                | 33             | 7.32  | 0.38 | 0.07 | 6.87       | 0.47 | 0.00 | 1.73       | 1.52 | 0.90 | 2.08       | 0.43 | 0.00 | 2.26       | 1.46 | 0.37 |
| 100                | 10             | 6.46  | 0.83 | 0.26 | 12.87      | 0.76 | 0.01 | 2.02       | 1.73 | 0.82 | 1.98       | 0.31 | 0.00 | 2.88       | 2.37 | 1.23 |
| 67                 | 67             | 0.00  | 0.00 | 0.00 | 0.00       | 0.00 | 0.00 | 0.00       | 0.00 | 0.00 | 1.61       | 0.83 | 0.00 | 0.01       | 0.00 | 0.00 |
| 67                 | 50             | 0.57  | 0.00 | 0.00 | 4.75       | 0.00 | 0.00 | 3.42       | 2.16 | 0.00 | 1.88       | 0.36 | 0.00 | 3.27       | 2.47 | 0.03 |
| 67                 | 33             | 0.80  | 0.22 | 0.00 | 8.22       | 0.23 | 0.00 | 1.33       | 0.99 | 0.19 | 1.39       | 0.37 | 0.00 | 2.25       | 1.86 | 0.60 |
| 67                 | 10             | 6.16  | 0.48 | 0.27 | 10.45      | 0.44 | 0.00 | 1.57       | 1.23 | 0.60 | 0.94       | 0.15 | 0.00 | 2.74       | 2.18 | 0.73 |
| 33                 | 33             | 0.26  | 0.00 | 0.00 | 0.01       | 0.00 | 0.00 | 3.25       | 2.23 | 0.08 | 0.33       | 0.04 | 0.00 | 0.00       | 0.00 | 0.00 |
| 33                 | 10             | 5.49  | 0.34 | 0.23 | 9.23       | 0.09 | 0.00 | 2.78       | 2.11 | 0.15 | 1.03       | 0.16 | 0.00 | 1.44       | 1.16 | 0.45 |

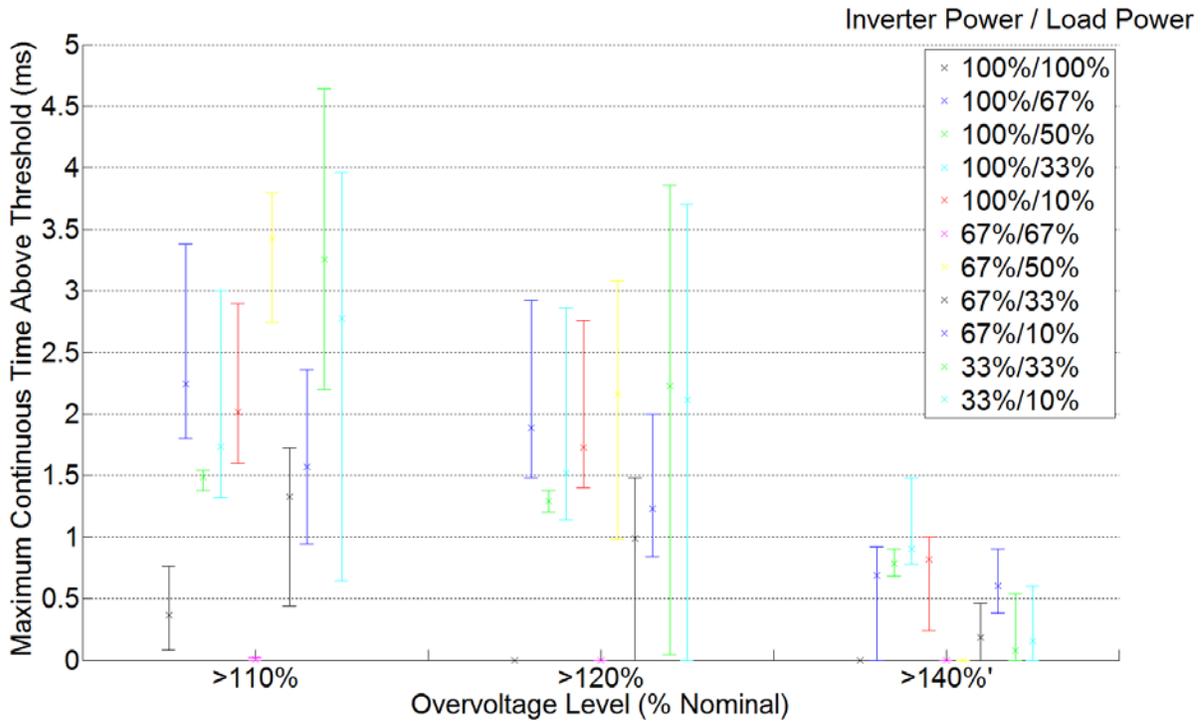
**Table 5: Maximum (top) and average (bottom) of the maximum continuous time above a given voltage threshold**

A plot of the maximum continuous over-voltage duration ranges for Inverter 2 is shown in Figure 10. The largest measured continuous over-voltage duration above 110% of nominal was 15.92 ms. The voltage duration times tended to increase with increasing load ratio and this inverter spent very little time above the 120% and 140% thresholds.



**Figure 10: Maximum continuous over-voltage duration times for Inverter 2**

A plot of the maximum continuous over-voltage duration ranges for Inverter 3 is shown in Figure 11. The largest measured continuous over-voltage duration above 110% of nominal was 4.64 ms. This inverter had consistently short continuous over-voltage times, but did dwell a similar amount of time above the 120% and 140% thresholds as the 110% threshold.



**Figure 11: Maximum continuous over-voltage duration times for Inverter 3**

A plot of the maximum continuous over-voltage duration ranges for Inverter 4 is shown in Figure 12. The largest measured continuous over-voltage duration above 110% of nominal was 4.60 ms. This inverter also had consistently short continuous over-voltage times. It was capable of dwelling above 120% of nominal for a similar amount of time as 110% of nominal, but spent very little time above the 140% threshold.

A plot of the maximum continuous over-voltage duration ranges for Inverter 5 is shown in Figure 13. The largest measured continuous over-voltage duration above 110% of nominal was 5.38 ms. This inverter had consistently short continuous over-voltage times, but did dwell a similar amount of time above the 120% and 140% thresholds as the 110% threshold.

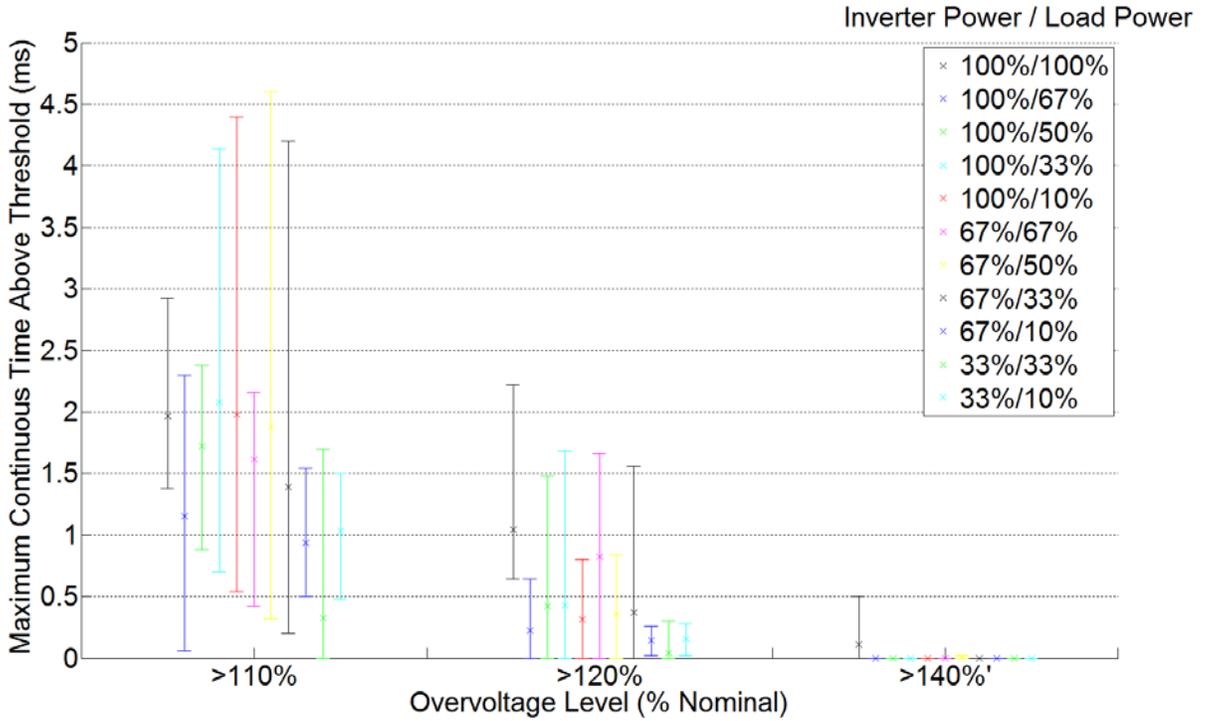


Figure 12: Maximum continuous over-voltage duration times for Inverter 4

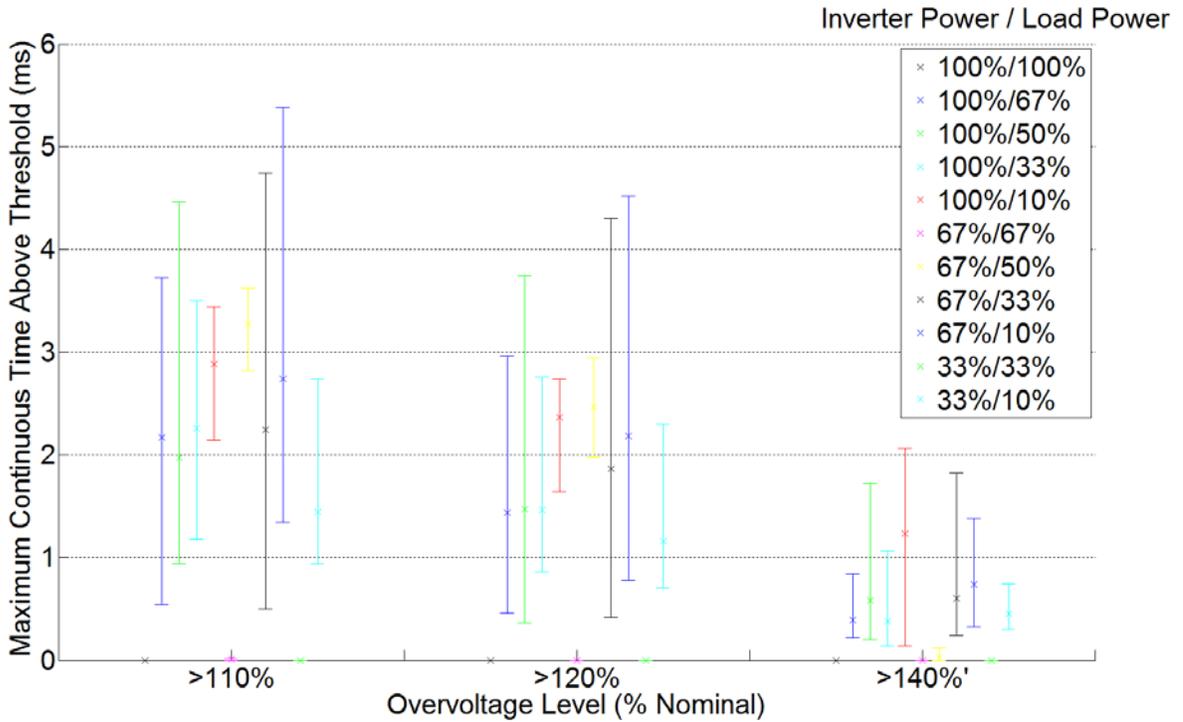


Figure 13: Maximum continuous over-voltage duration times for Inverter 5

### 3.3 Maximum Instantaneous Over-voltage

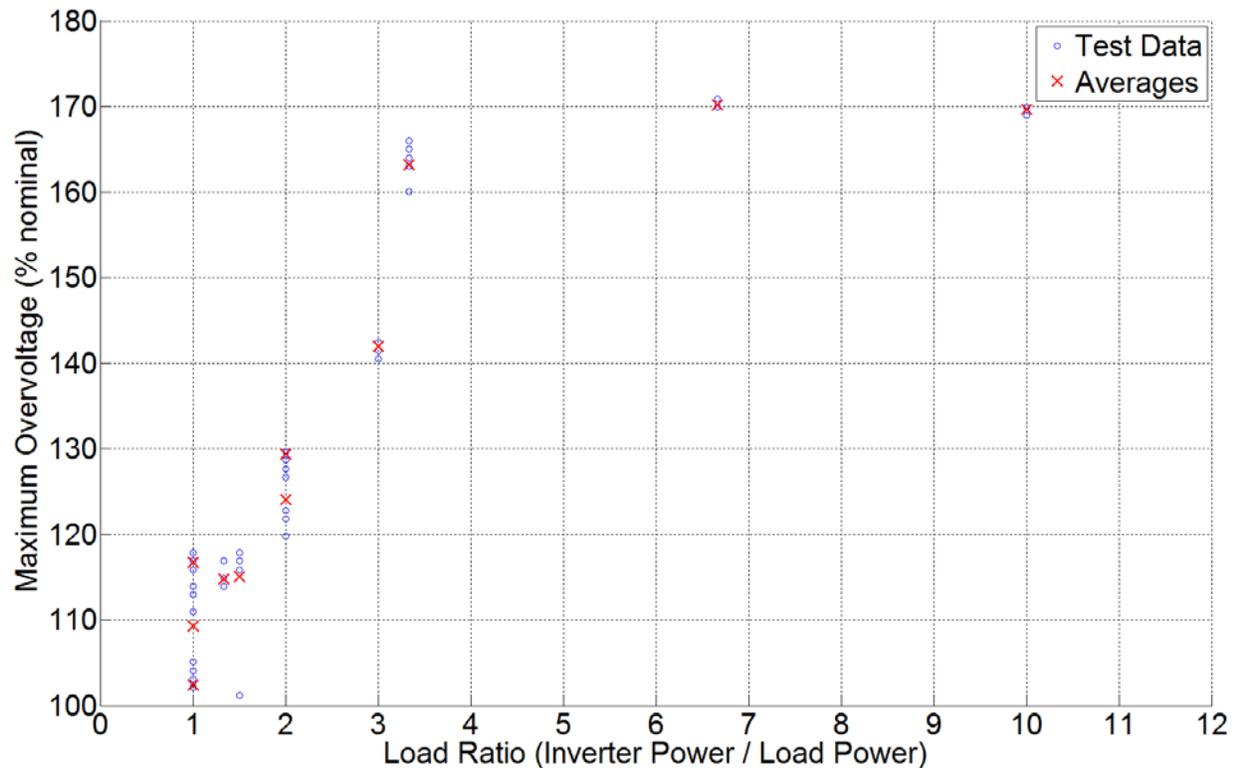
This section shows data about the maximum instantaneous over-voltage measurement recorded at any point during the transient event. Averages and maximums across seven different tests at each load setting are provided in Table 6. The plots in the following two sections display the parameter of interest as a function of load ratio, which is defined as the inverter output power divided by the load power. Each plot shows the average across all seven tests at a given load ratio (red “X”) as well as the individual test data points (blue circles). Note that some load ratios have more than one averaged data point but occur at different power outputs (e.g. 100%/100% and 67%/67% inverter/load power both have a load ratio of 1.0).

**Table 6: Maximum (top) and average (bottom) of the maximum instantaneous voltage measurement**

| Maximum Instantaneous Voltage (% Nominal) |                |            |            |            |            |            |
|---|----------------|------------|------------|------------|------------|------------|
| Inverter Power (%)                        | Load Power (%) | Inverter 1 | Inverter 2 | Inverter 3 | Inverter 4 | Inverter 5 |
| 100                                       | 100            | 113.9      | 106.9      | 113.1      | 149.7      | 109.9      |
| 100                                       | 67             | 117.9      | 120.2      | 154.0      | 136.9      | 151.1      |
| 100                                       | 50             | 127.7      | 126.9      | 159.1      | 131.0      | 163.9      |
| 100                                       | 33             | 142.4      | 133.6      | 170.9      | 132.3      | 156.0      |
| 100                                       | 10             | 169.9      | 151.6      | 190.5      | 128.4      | 196.3      |
| 67  | 67             | 103.1      | 106.1      | 110.8      | 132.7      | 111.9      |
| 67  | 50             | 116.9      | 116.3      | 131.6      | 140.3      | 145.2      |
| 67  | 33             | 129.6      | 126.1      | 152.0      | 134.4      | 160.9      |
| 67  | 10             | 170.9      | 136.7      | 167.0      | 125.9      | 184.5      |
| 33  | 33             | 117.9      | 111.6      | 162.2      | 126.7      | 109.9      |
| 33  | 10             | 166.0      | 124.1      | 175.6      | 128.4      | 161.9      |

| Average Maximum Instantaneous Voltage (% Nominal) |                |            |            |            |            |            |
|---|----------------|------------|------------|------------|------------|------------|
| Inverter Power (%)                                | Load Power (%) | Inverter 1 | Inverter 2 | Inverter 3 | Inverter 4 | Inverter 5 |
| 100   | 100            | 109.3      | 106.0      | 112.1      | 138.0      | 107.9      |
| 100   | 67             | 115.0      | 116.5      | 145.6      | 122.4      | 149.9      |
| 100   | 50             | 124.0      | 119.5      | 156.5      | 125.7      | 156.7      |
| 100   | 33             | 142.0      | 129.0      | 161.1      | 125.1      | 151.6      |
| 100   | 10             | 169.6      | 139.3      | 169.7      | 124.5      | 175.0      |
| 67  | 67             | 102.4      | 105.4      | 109.4      | 127.2      | 110.1      |
| 67  | 50             | 114.8      | 116.0      | 128.4      | 127.4      | 139.8      |
| 67  | 33             | 129.4      | 121.9      | 141.1      | 122.2      | 156.3      |
| 67  | 10             | 170.2      | 131.7      | 156.8      | 123.4      | 164.3      |
| 33  | 33             | 116.7      | 107.1      | 132.3      | 113.8      | 109.4      |
| 33  | 10             | 163.2      | 122.5      | 142.4      | 123.4      | 157.6      |

The maximum instantaneous over-voltages measured as a function of load ratio for Inverter 1 are found in Figure 14. The maximum voltage measured during any of the tests of Inverter 1 was 170.9% of nominal (note: this could also be phrased as 70.9% *above* nominal). As expected, there is a general trend of higher instantaneous voltage measurements at higher load ratios. This inverter had relatively low variance in over-voltage level across multiple tests.



**Figure 14: Maximum instantaneous over-voltage vs. load ratio for Inverter 1**

The maximum instantaneous over-voltages measured as a function of load ratio for Inverter 2 are found in Figure 15. The maximum voltage measured during any of the tests of Inverter 2 was 151.6% of nominal in one case, while no other tests exceeded 140% of nominal. Inverter 2 had among the lowest instantaneous over-voltage levels of all the test inverters. There is a general trend of higher instantaneous voltage measurements at higher load ratios.

The maximum instantaneous over-voltages measured as a function of load ratio for Inverter 3 are found in Figure 16. The maximum voltage measured during any of the tests of Inverter 3 was 190.5% of nominal. Inverter 3 had more variability in maximum voltage between tests, and also had a general trend of higher instantaneous voltage measurements at higher load ratios.

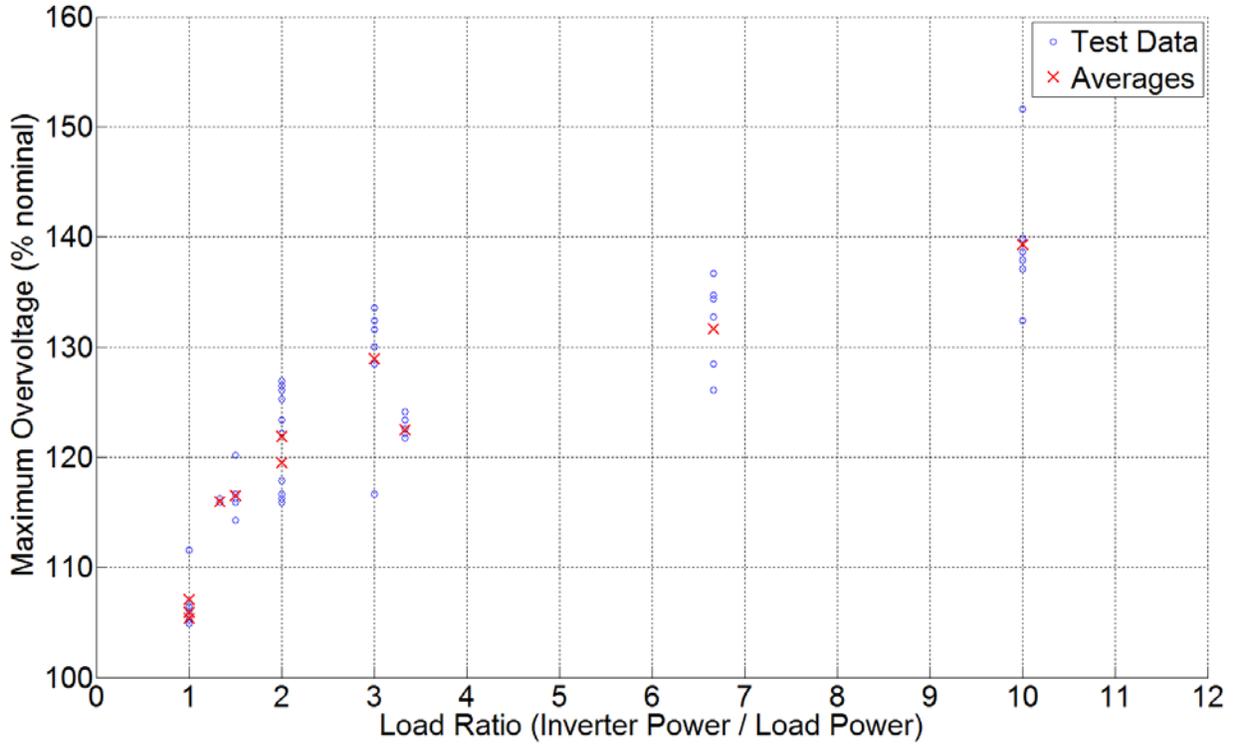


Figure 15: Maximum instantaneous over-voltage vs. load ratio for Inverter 2

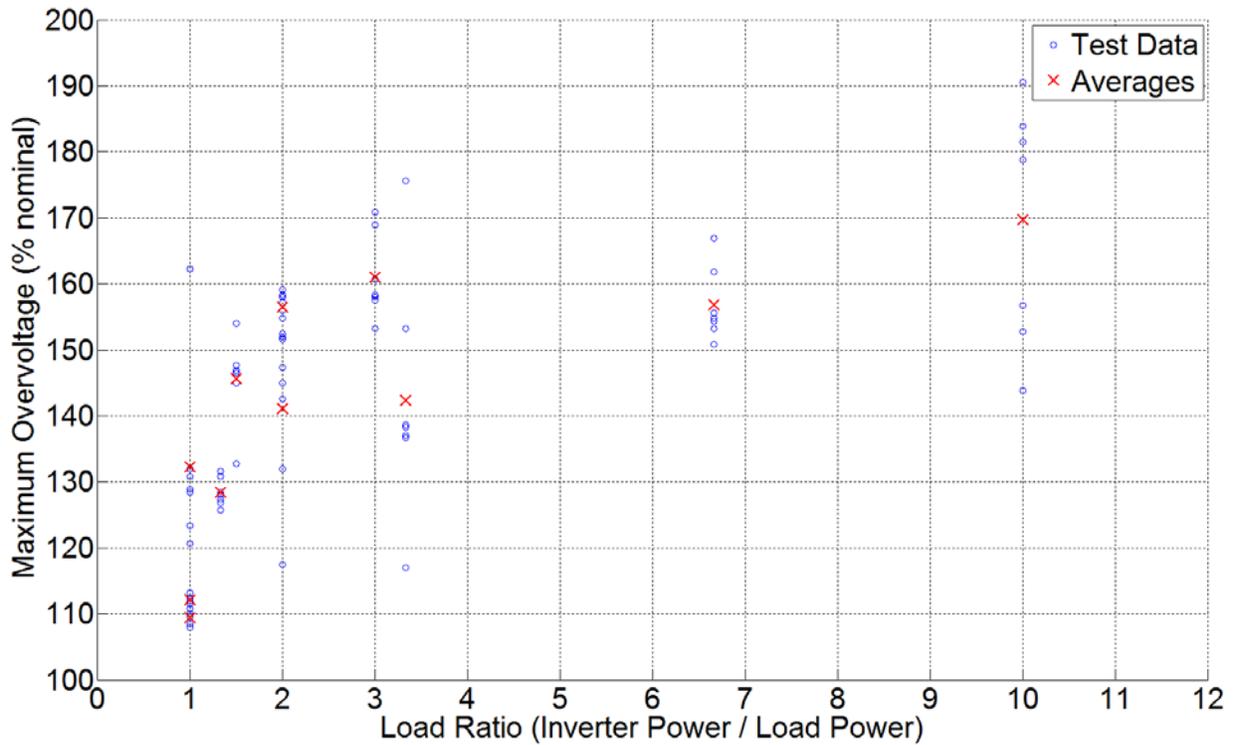
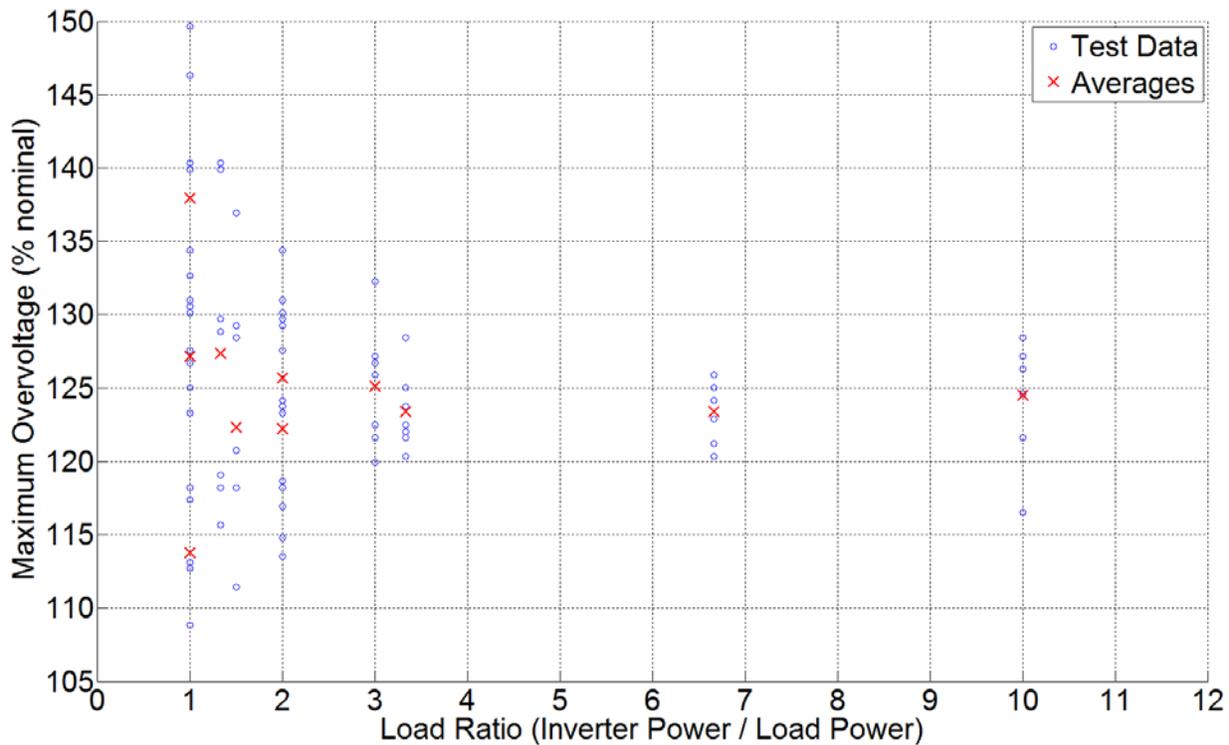


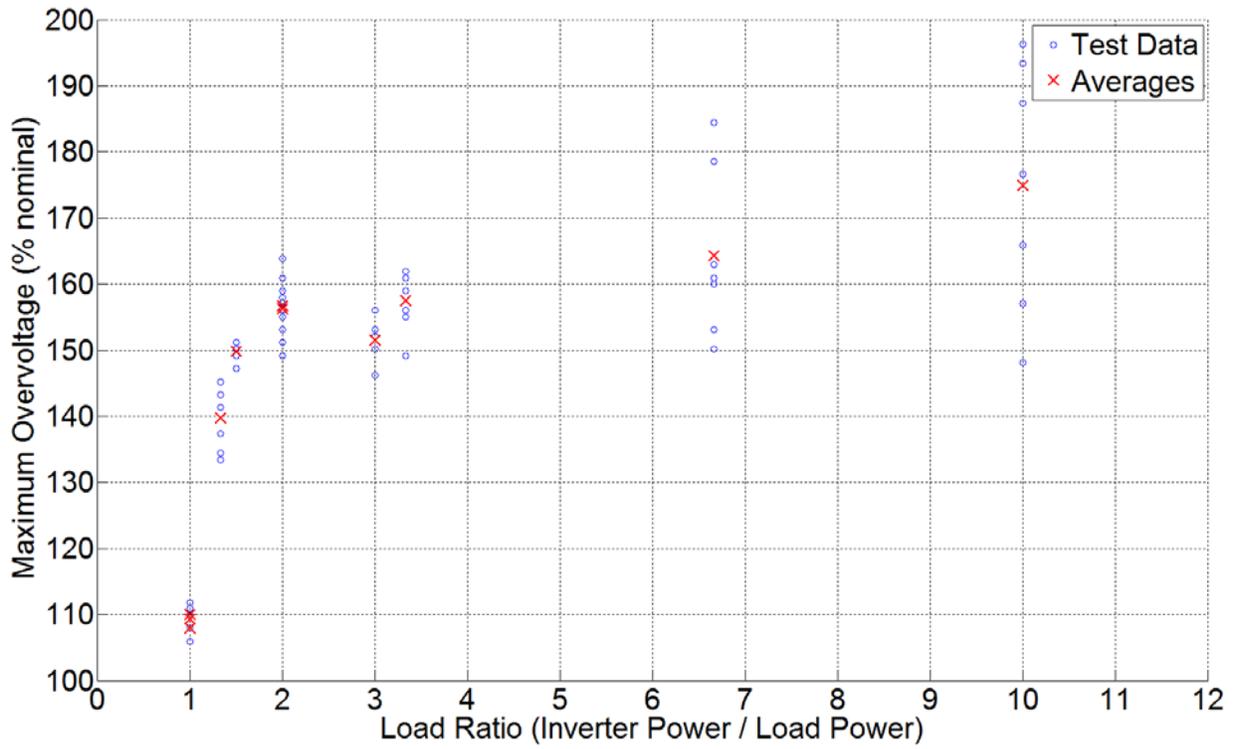
Figure 16: Maximum instantaneous over-voltage vs. load ratio for Inverter 3

The maximum instantaneous over-voltages measured as a function of load ratio for Inverter 4 are found in Figure 17. The maximum voltage measured during any of the tests of Inverter 4 was 149.7% of nominal. This maximum voltage occurred during a 1:1 load ratio test, somewhat surprisingly. This appears to be because all three phase voltages drift in a positive direction after the grid disconnects, and the drifting lasted longer (and hence reached higher overvoltages) for 1:1 load ratio, possibly because dv/dt trip settings were not activated, if present. Along with Inverter 2, Inverter 4 consistently had lower maximum voltage measurements across the entire range of load ratios. There does not appear to be a correlation between load ratio and the maximum over-voltage level for Inverter 4.

The maximum instantaneous over-voltages measured as a function of load ratio for Inverter 5 are found in Figure 18. The maximum voltage measured during any of the tests of Inverter 5 was 196.3% of nominal. Inverter 5 had more variability in maximum voltage as load ratio increases, and also had the general trend of higher instantaneous voltage measurements at higher load ratios.



**Figure 17: Maximum instantaneous over-voltage vs. load ratio for Inverter 4**



**Figure 18: Maximum instantaneous over-voltage vs. load ratio for Inverter 5**

### 3.4 Trip Time / Time to Disconnect

This section shows data about the trip time – or time to disconnect – for each test inverter as a function of load ratio. For the purposes of this testing, the trip time was defined as the time from switch S3 opening (see Figure 1) until the time that each phase voltage ceased to exceed a predefined threshold of 30V. In many cases, there was very little export of current from the test inverter by this time, but the trip time was based off of AC terminal voltage. Averages and maximums across seven different tests at each load setting are provided in Table 7. With the exception of one anomalous test run which is discussed later in this report, it can be seen that no inverters exceeded a trip time of two seconds, which is the maximum time an IEEE 1547 compliant inverter can remain connected to an islanded system. (The anomalous run has not been included in this table.)

**Table 7: Maximum (top) and average (bottom) time to disconnect for all inverters**

| Maximum Trip Time (ms) |                |            |            |            |            |            |
|------------------------|----------------|------------|------------|------------|------------|------------|
| Inverter Power (%)     | Load Power (%) | Inverter 1 | Inverter 2 | Inverter 3 | Inverter 4 | Inverter 5 |
| 100                    | 100            | 1262.4     | 114.0      | 163.6      | 805.2      | 7.6        |
| 100                    | 67             | 224.1      | 153.3      | 9.2        | 725.9      | 13.3       |
| 100                    | 50             | 721.6      | 197.7      | 7.8        | 788.4      | 23.3       |
| 100                    | 33             | 88.2       | 166.5      | 7.4        | 770.0      | 49.3       |
| 100                    | 10             | 89.6       | 124.4      | 46.2       | 588.6      | 180.5      |
| 67                     | 67             | 1068.6     | 120.5      | 180.6      | 805.6      | 7.6        |
| 67                     | 50             | 902.7      | 135.8      | 81.2       | 757.1      | 9.2        |
| 67                     | 33             | 223.8      | 272.6      | 20.0       | 467.7      | 25.0       |
| 67                     | 10             | 81.8       | 137.6      | 44.6       | 525.5      | 93.1       |
| 33                     | 33             | 979.2      | 156.3      | 201.0      | 511.3      | 7.2        |
| 33                     | 10             | 98.1       | 101.3      | 35.2       | 602.2      | 9.0        |

| Average Trip Time (ms) |                |            |            |            |            |            |
|------------------------|----------------|------------|------------|------------|------------|------------|
| Inverter Power (%)     | Load Power (%) | Inverter 1 | Inverter 2 | Inverter 3 | Inverter 4 | Inverter 5 |
| 100                    | 100            | 865.8      | 86.1       | 149.0      | 636.4      | 6.5        |
| 100                    | 67             | 186.2      | 129.2      | 6.8        | 506.6      | 7.0        |
| 100                    | 50             | 273.2      | 179.0      | 4.5        | 485.9      | 7.7        |
| 100                    | 33             | 76.9       | 103.3      | 5.8        | 401.1      | 20.8       |
| 100                    | 10             | 78.1       | 102.1      | 13.7       | 328.2      | 60.4       |
| 67                     | 67             | 770.7      | 98.1       | 159.0      | 560.8      | 6.1        |
| 67                     | 50             | 605.5      | 132.4      | 27.9       | 432.4      | 8.0        |
| 67                     | 33             | 116.1      | 187.3      | 11.9       | 303.3      | 9.7        |
| 67                     | 10             | 71.0       | 93.4       | 14.3       | 254.5      | 46.1       |
| 33                     | 33             | 497.1      | 124.8      | 45.8       | 270.5      | 5.7        |
| 33                     | 10             | 79.9       | 93.6       | 17.1       | 407.2      | 6.3        |

Individual plots of all test points and averages for trip times as a function of load ratio are shown in Figure 19 - Figure 23. Inverter 1 typically had the longest trip times, Inverter 4 had more moderate trip times, and both Inverters 2 and 3 had shorter trip times - typically less than ten AC cycles. Inverter 5 consistently had the shortest trip times. Inverters 1-3 generally had shorter trip times as load ratio increased, which is the expected result: higher generation to load ratios lead to faster over-voltages and hence faster tripping. In contrast, Inverter 4 did not seem to have a dependence on load ratio, and Inverter 5 appeared to have slightly higher trip times at higher load ratios, somewhat unexpectedly. This unexpected result is not concerning, however, especially given the very short trip times. None of the trip times shown violate anti-islanding requirements for grid-compliant inverters.

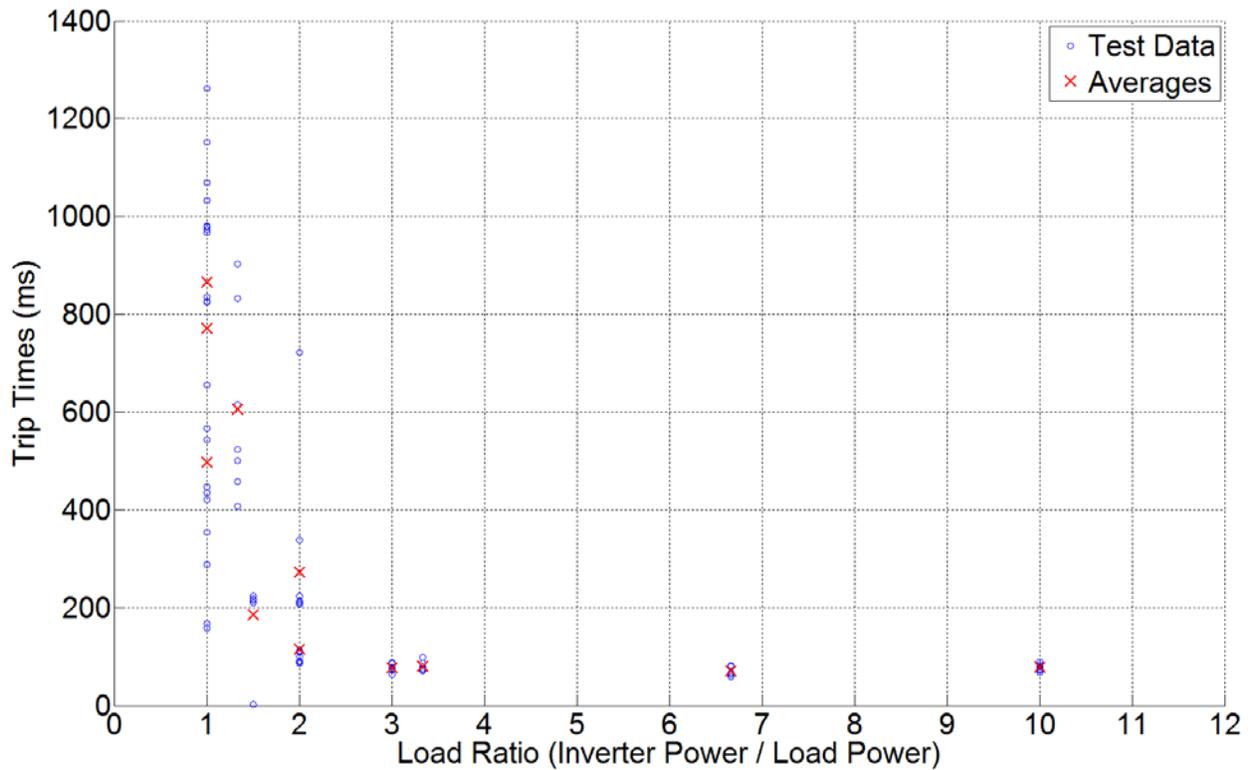


Figure 19: Trip time as a function of load ratio for Inverter 1

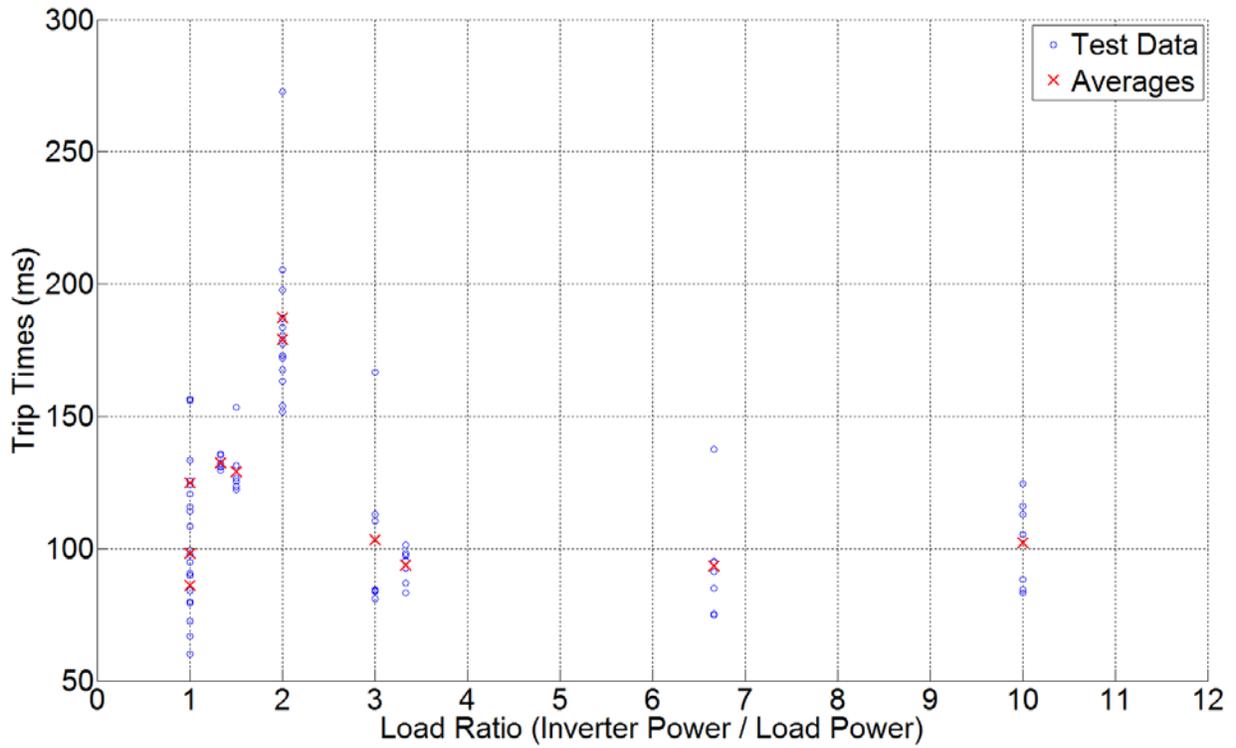


Figure 20: Trip time as a function of load ratio for Inverter 2

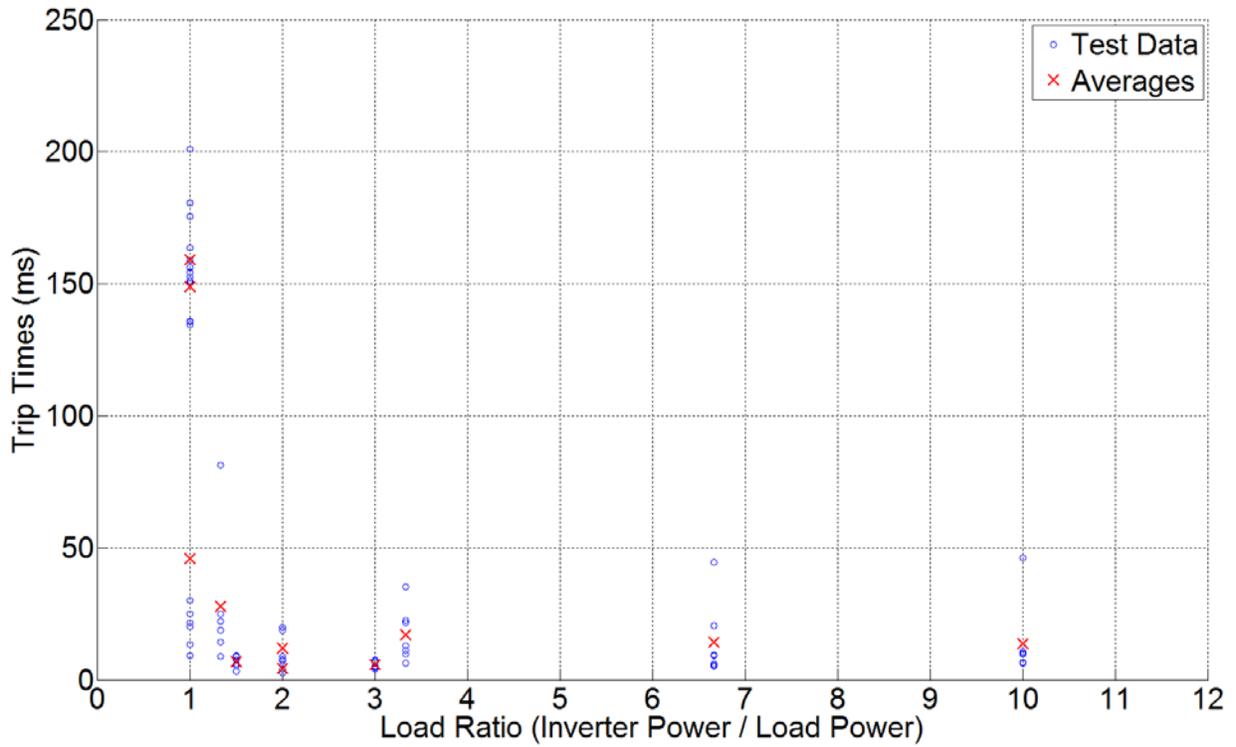


Figure 21: Trip time as a function of load ratio for Inverter 3



### 3.5 Waveforms of Interest

This section shows a selection of waveforms showing inverter behavior during the transient event for each of the test inverters. Each inverter had unique responses to the load rejection event, but the responses can be grouped into similar and repeatable response types. This section contains some waveforms that are considered typical inverter responses, along with others that had a unique, outlying, or particularly interesting response. This section is not meant to be an exhaustive report on all waveform characteristics, but instead is meant to provide insights into the differences between inverter responses.

Each waveform plot shows the AC terminal voltages, inverter current, DC bus voltage, and the trigger signal showing when switch S3 opened (see Figure 1). The opening of switch S3 occurs at time 0.75 seconds for every test. Each plot also has horizontal lines showing the 110%, 120%, and 140% voltage threshold levels (when necessary). The interval of time where the maximum continuous over-voltage at each voltage threshold occurs is highlighted in each waveform. The alphanumeric name given in parenthesis in each waveform caption corresponds to the raw data file name provided to SolarCity as part of this task.

Note that the AC current sensors used for Inverters 1, 2 and 3 are only capable of detecting AC current; hence some current waveforms are distorted somewhat, such that any DC and very low frequency components are suppressed.

#### *Inverter 1 Waveforms*

Figure 24 shows a typical response of Inverter 1 to unity or near unity load ratios. The inverter would typically output a sinusoidal waveform with a non-nominal voltage magnitude, often without any measured over-voltage. Figure 25 shows a more interesting but less common case where there are larger fluctuations in the sinusoidal magnitude before the inverter tripped. An even less common response is seen in Figure 26, where there was one large over-voltage spike in an otherwise sinusoidal response, leading to immediate shut down.

Figure 27 shows a mixed response that was more typical at intermediate load ratios. The output waveform was mostly sinusoidal, but there were initially some half cycles that were clipped near the DC bus voltage, indicating over-modulation. High load ratio responses were characterized by a square wave output that appeared to clip at a threshold (after an overshoot event), indicating hard over-modulation, and reversed polarity at roughly the AC line cycle frequency, as seen in Figure 28.

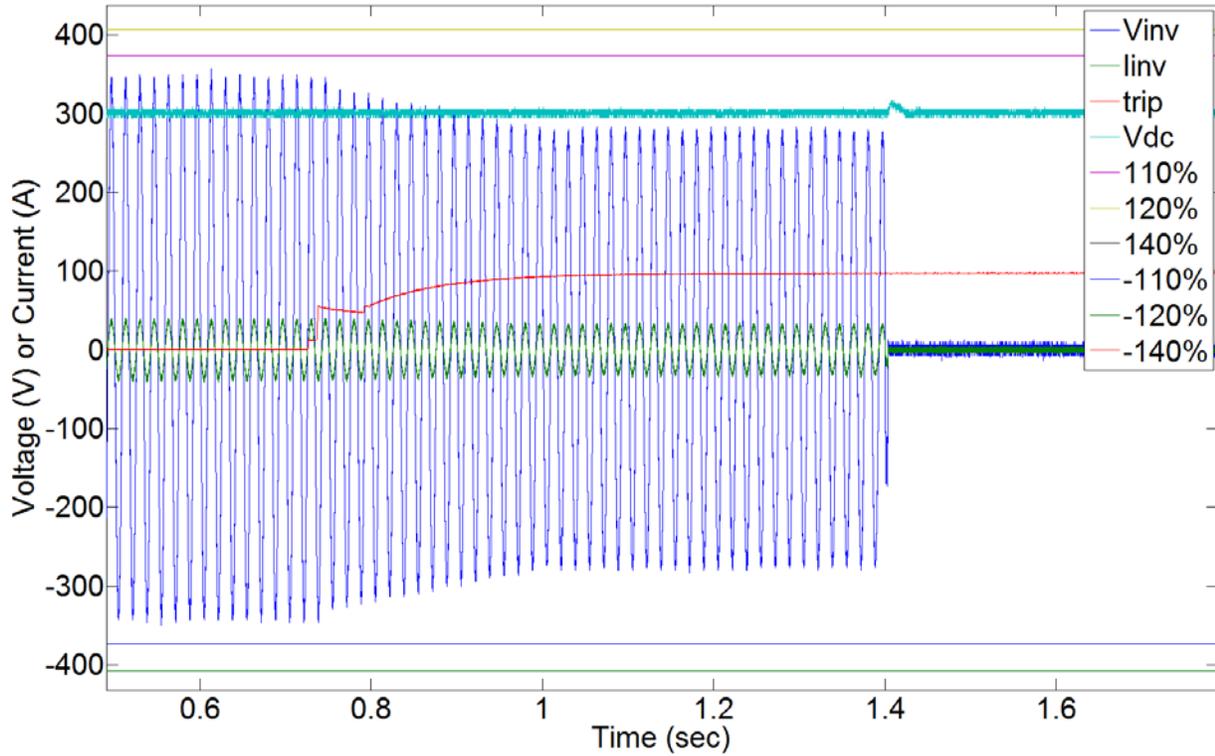


Figure 24: Inverter 1 waveform at unity load ratio – 100% power (T11\_0001)

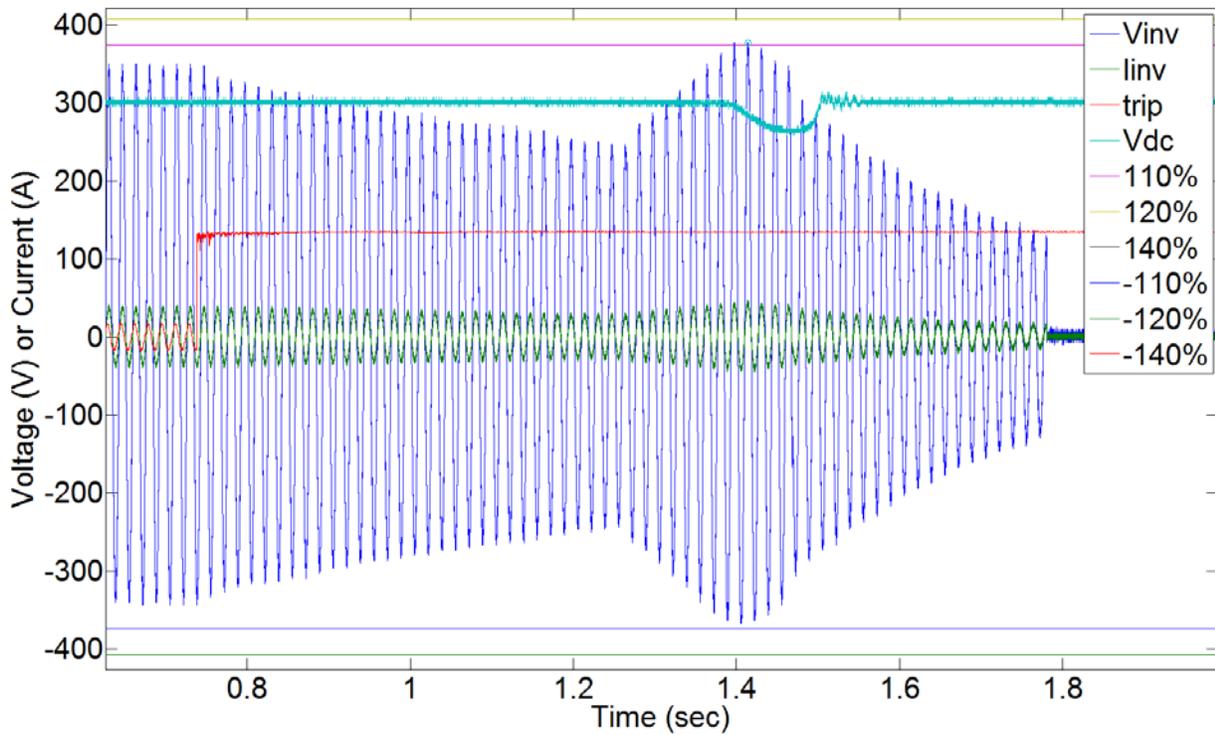


Figure 25: Inverter 1 waveform at unity load ratio – 100% power (T11\_0006)

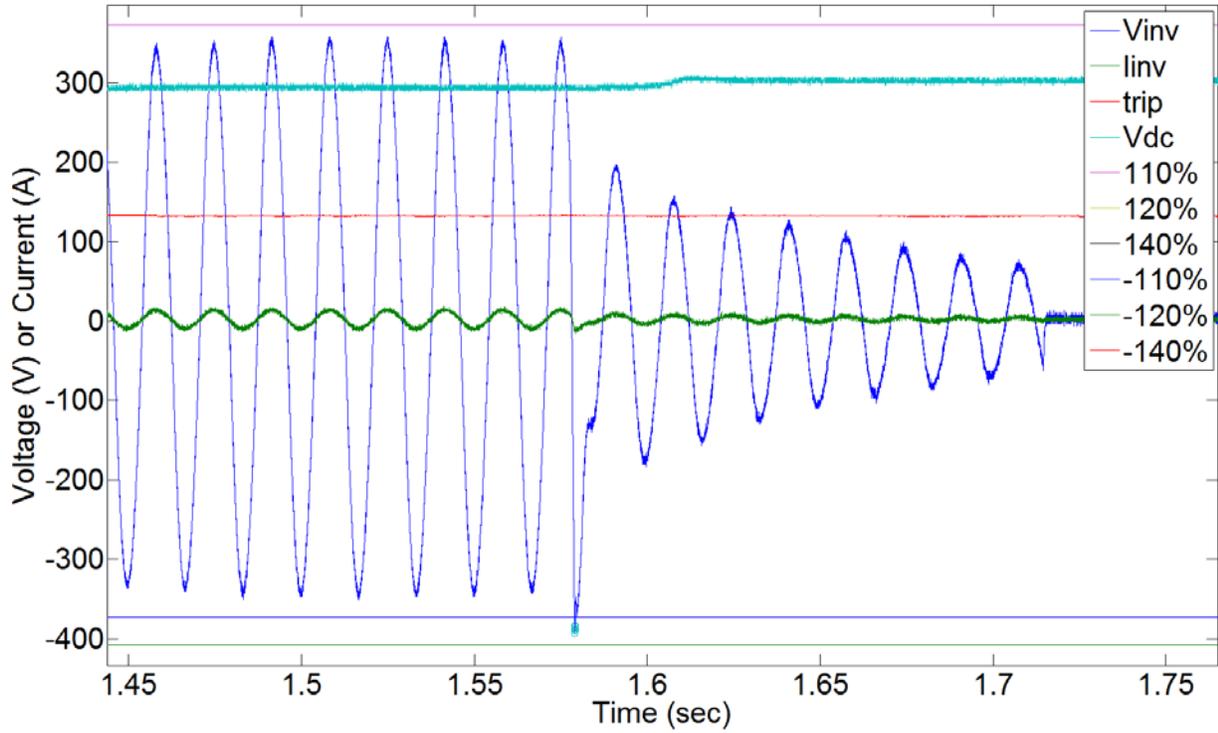


Figure 26: Inverter 1 waveform at unity load ratio - 33% power (T33\_0000)

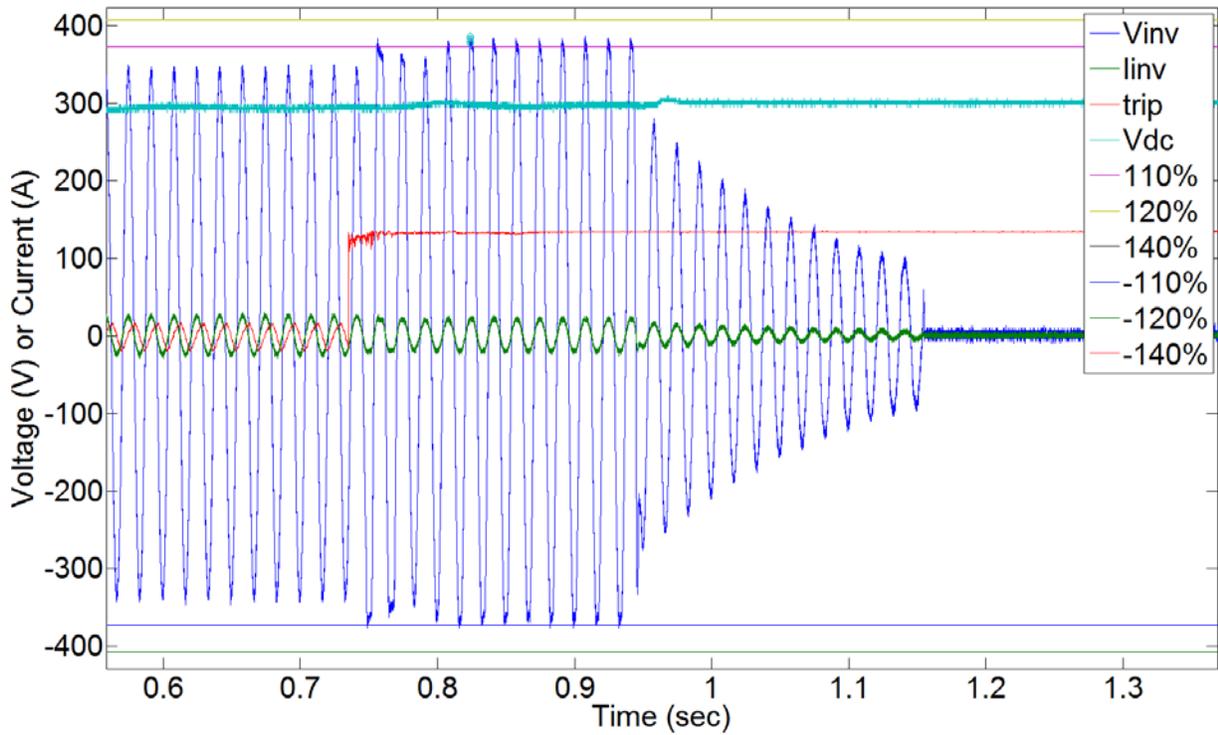


Figure 27: Inverter 1 waveform at medium load ratio - 67% inverter / 50% load power (T56\_0018)

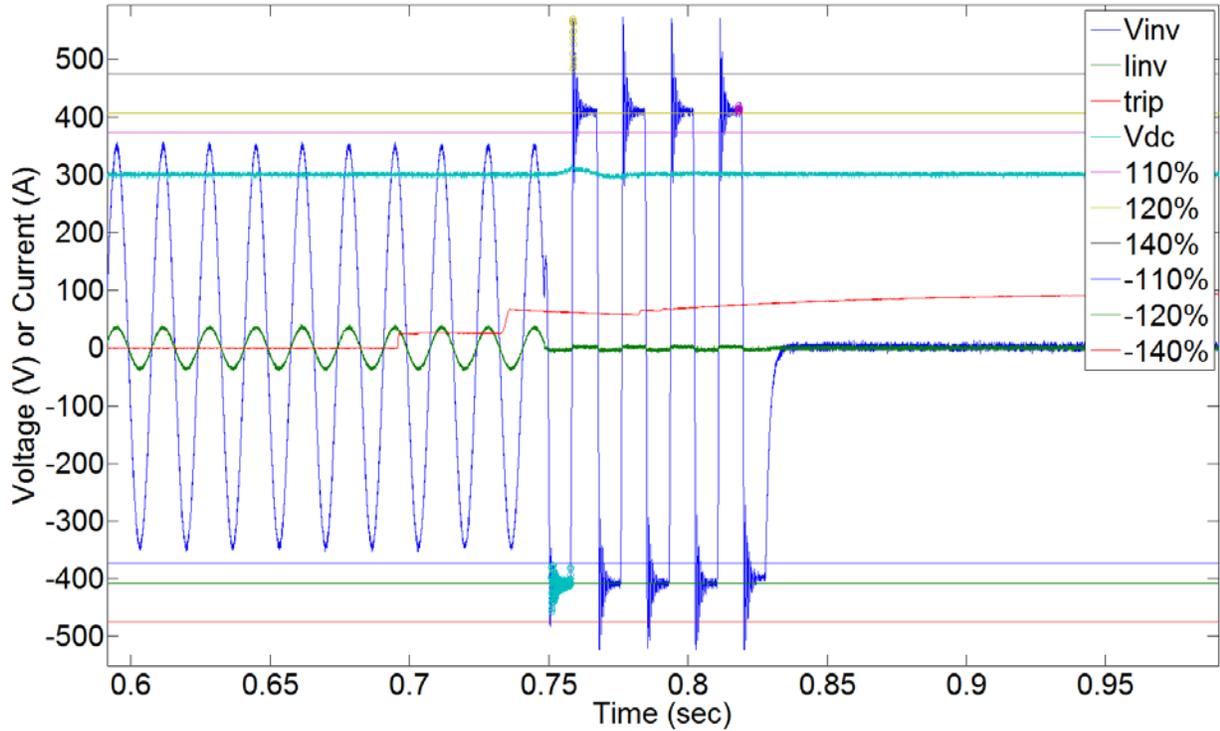


Figure 28: Inverter 1 waveform at high load ratio – 100% inverter / 10% load power (T01\_0000)

### ***Inverter 2 Waveforms***

Figure 29 shows a typical response of Inverter 2 unity load ratios; the output was typically sinusoidal for a handful of cycles at slightly higher than nominal voltage with little or no over-voltage recorded. At greater than unity load ratios, the output would be a clipped sinusoid, roughly following the AC half cycle, as seen in Figure 30. This probably indicates over-modulation. Since the output appeared to clip at the DC input supply voltage, additional testing with variable DC input voltage was completed, as discussed in the next section.

Figure 31 shows a less common, but interesting waveform at intermediate load ratio that had mixed sinusoidal and square wave (or clipped sinusoidal) response. This waveform appeared to be a transition to what was observed at medium to high load ratios, as seen in Figure 32. At these higher load ratios, the response was typically an irregular square wave that was limited to the DC bus voltage (over-modulation), as well as intermediate cutoff voltage levels that cause the overall waveform to lose some of its periodicity.

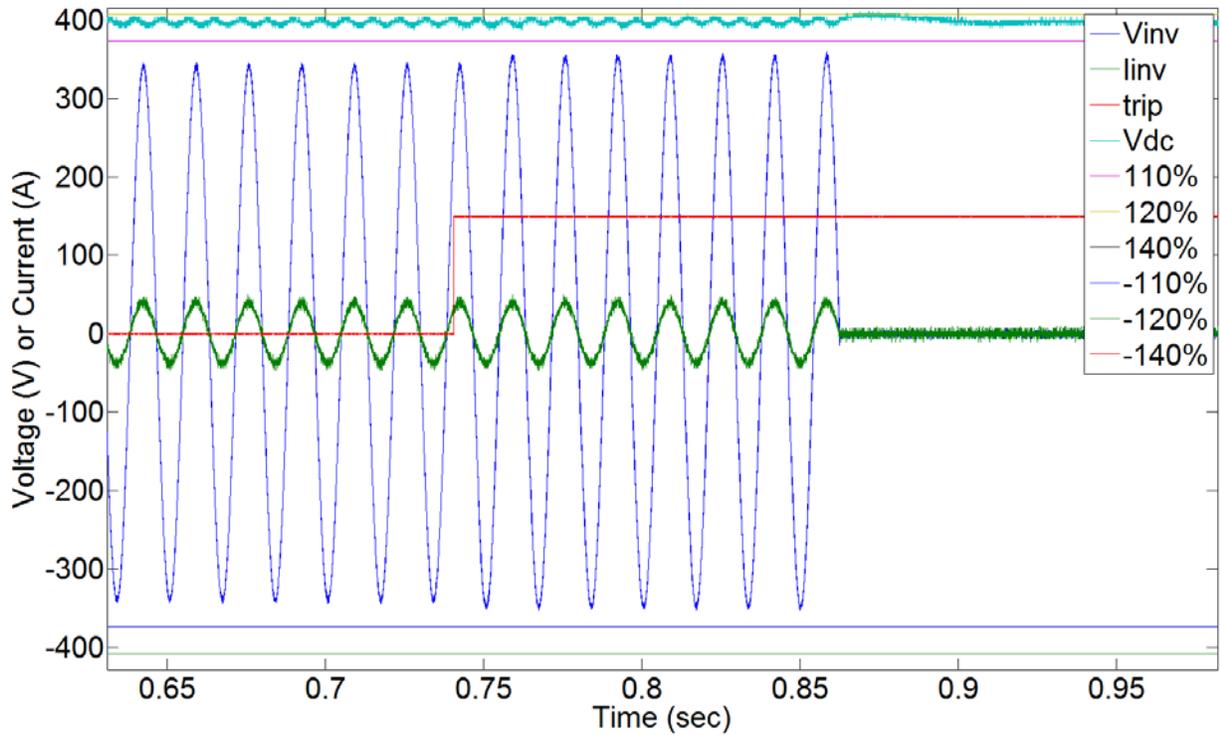


Figure 29: Inverter 2 waveform at unity load ratio – 100% power (E11\_0005)

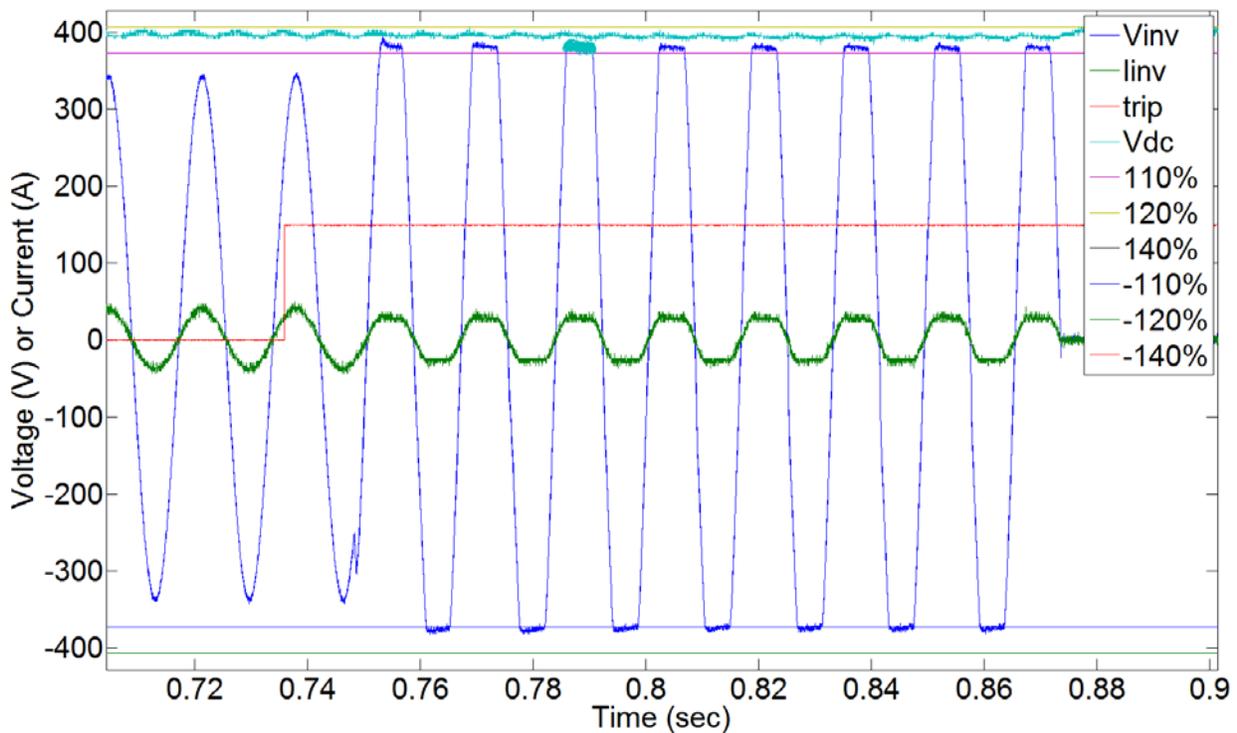
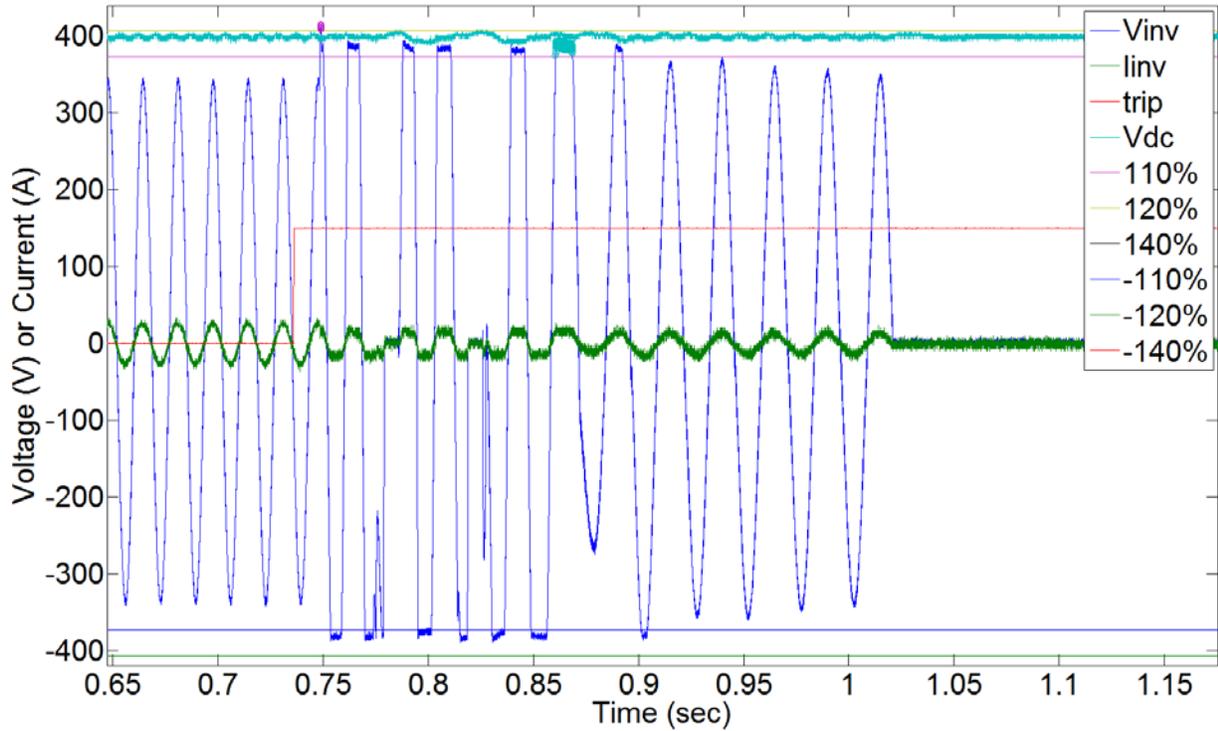
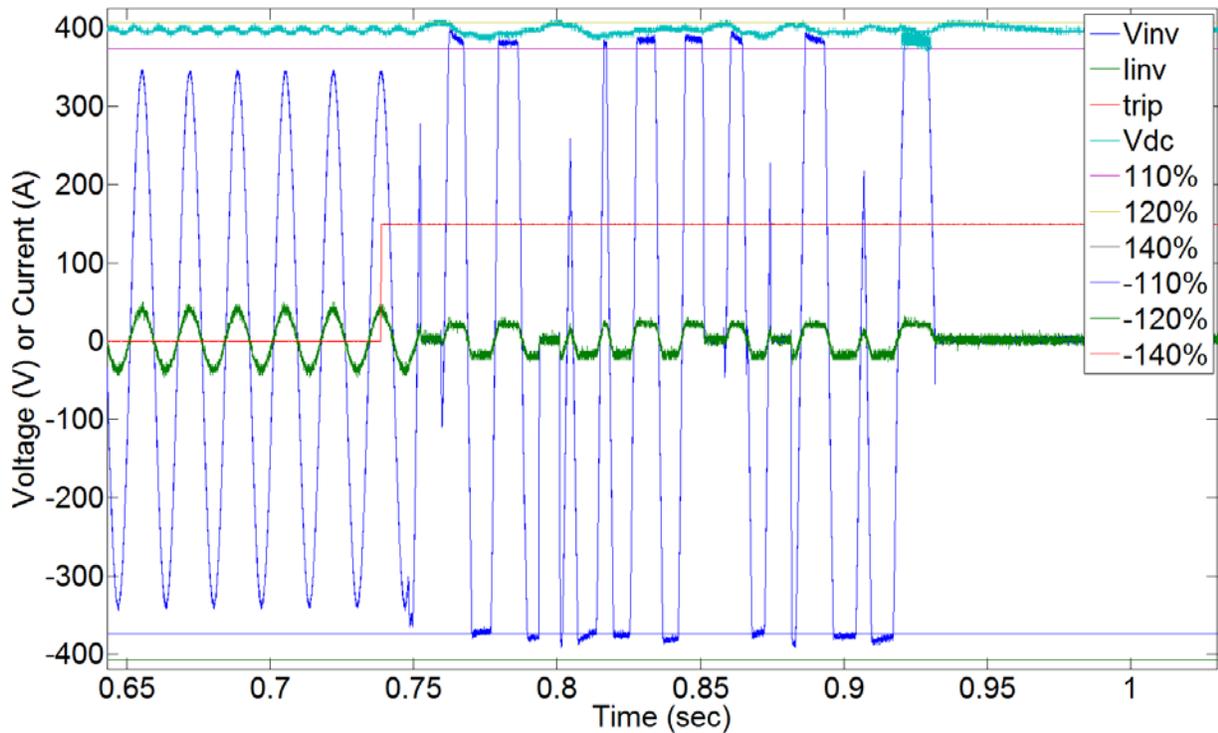


Figure 30: Inverter 2 waveform at medium load ratio – 100% inverter / 67% load power (E61\_0005)



**Figure 31: Inverter 2 waveform at medium/high load ratio – 67% inverter / 33% load power (E36\_0000)**



**Figure 32: Inverter 2 waveform at medium/high load ratio – 100% inverter / 50% load power (E51\_0000)**

One anomalous test result occurred on Inverter 2 that was omitted from the test results previously reported. Immediately after switch S3 opened, the inverter responded with the irregular square wave that was typical for medium to high load ratios. After several AC cycles, the measured terminal voltage remained at roughly the negative DC input voltage with a high frequency component superimposed. This behavior continued for the entire data capture window that concluded >4 seconds after the initial transient event. It is unclear when this voltage level ceased to persist at the AC terminals.

It is unclear if this result was due to problems with the inverter controls, the test equipment, or the measurement equipment. This test setting was repeated over 30 times in total, and the behavior could not be replicated. Since this test result is unexplained to date, it was not included in the data analysis presented in the previous sections. This test result is currently under investigation with the inverter manufacturer.

### ***Inverter 3 Waveforms***

Figure 33 shows a typical response of Inverter 3 at unity load ratio; it output a sinusoidal signal for a handful of AC cycles before shutting down. The waveform was typically slightly greater than nominal voltage with some oscillations in magnitude, and little or no over-voltage was recorded. At medium load ratios, the inverter would typically shut down very quickly after a single over-voltage spike shortly after the transient event, as seen in Figure 34. At the highest load ratio of 10:1, the inverter would similarly shut down very quickly after a single over-voltage spike, but also had some high frequency switching events, as seen in Figure 35 and Figure 36. The over-voltage measured in Figure 35 was the worst case over-voltage for this inverter, but lasted a very short amount of time. Figure 37 is the outlier for this inverter, as it stayed connected significantly longer than any other test case. The high-frequency voltage content in Figures 35 through 37 is not easily explained. It is worth noting that this inverter model is several years older than the others tested.

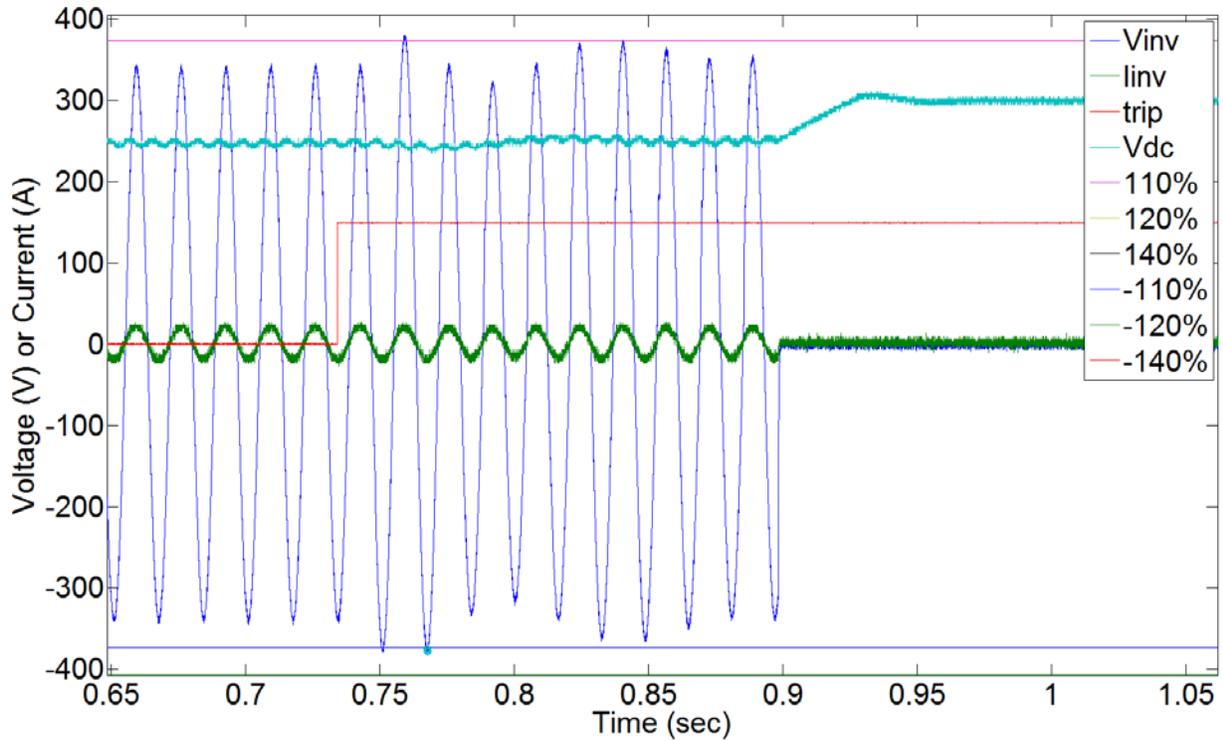


Figure 33: Inverter 3 waveform at unity load ratio - 100% power (S11\_0000)

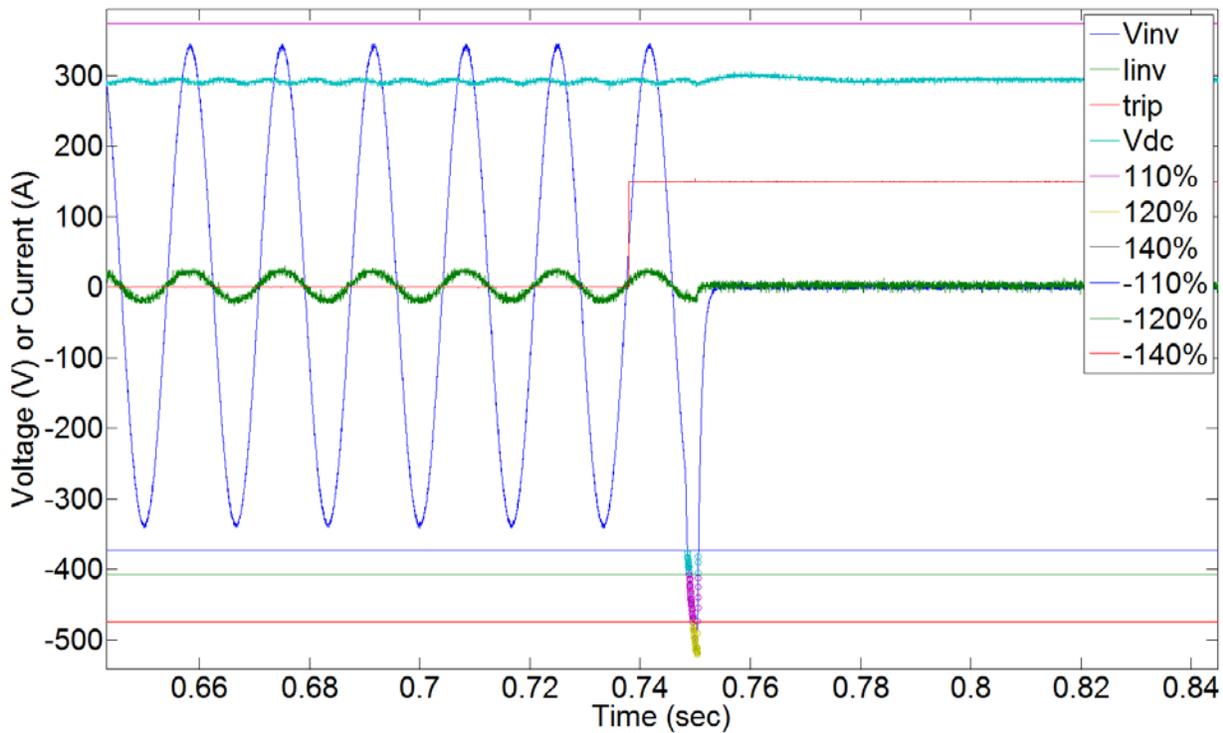


Figure 34: Inverter 3 waveform at medium load ratio - 100% inverter / 33% load power (S31\_0000)

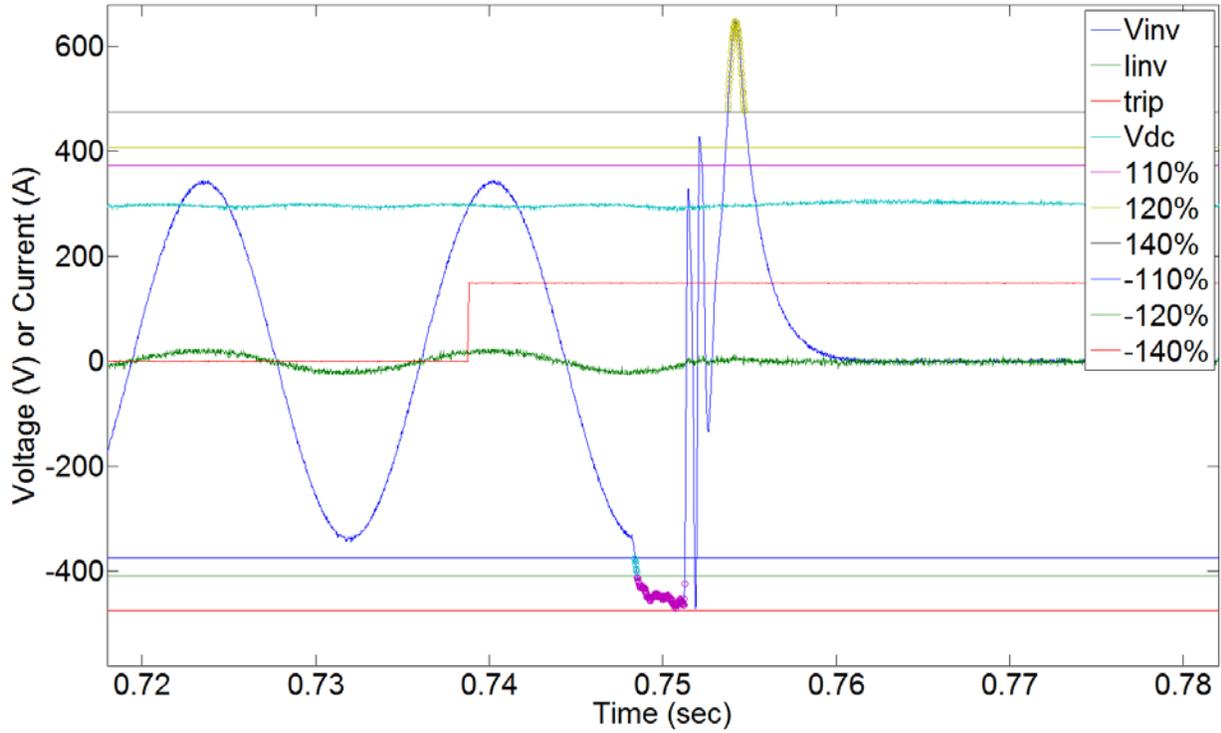


Figure 35: Inverter 3 waveform at high load ratio - 100% inverter / 10% load power (S01\_0006)

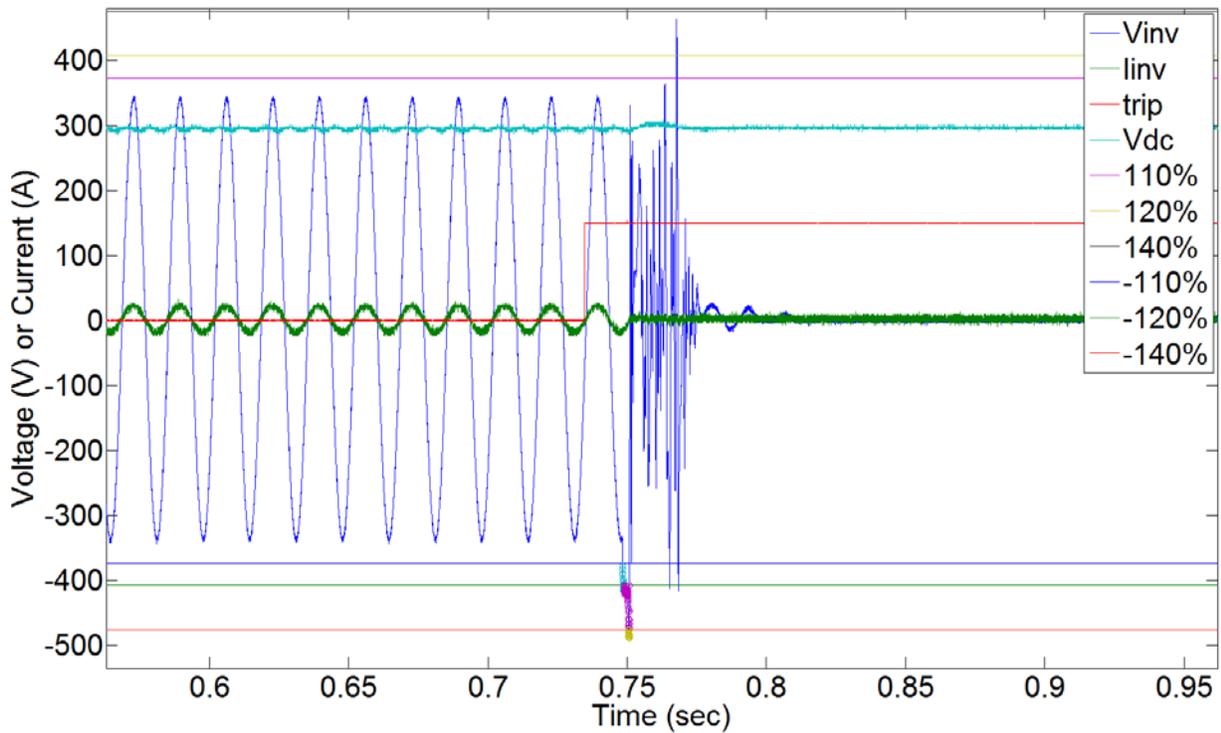


Figure 36: Inverter 3 waveform at high load ratio - 100% inverter / 10% load power (S01\_0004)

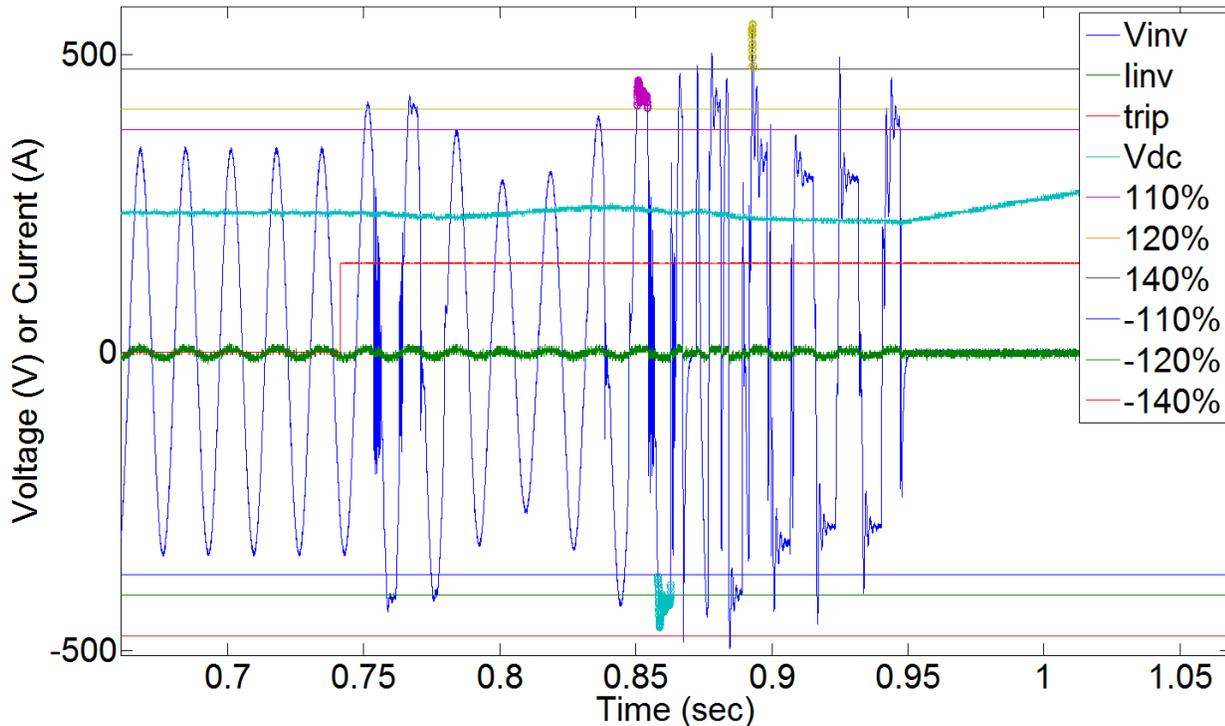


Figure 37: Inverter 3 waveform at unity load ratio – 33% power (S33\_0002)

### *Inverter 4 Waveforms*

Inverter 4 had a similar response across the entire range of load ratios, which partially explains the lack of clear trends in over-voltage time and magnitudes discussed in previous sections. Figure 38 shows a typical response across many load ratios; the inverter would attempt to balance the three phases for a couple of AC cycles before quickly shutting down after an over-voltage spike. This same behavior was observed for other load ratios in Figure 39 - Figure 41. The more interesting behavior observed in these waveforms was that the inverter held the output at an intermediate DC voltage level for a couple of AC cycles before disconnecting from the AC terminals. In some test cases – at a variety of loading levels – this inverter would switch back on after a short delay, as seen in Figure 41. The behavior seen in this particular waveform is the worst case in terms of the magnitude and duration of the late switching event.

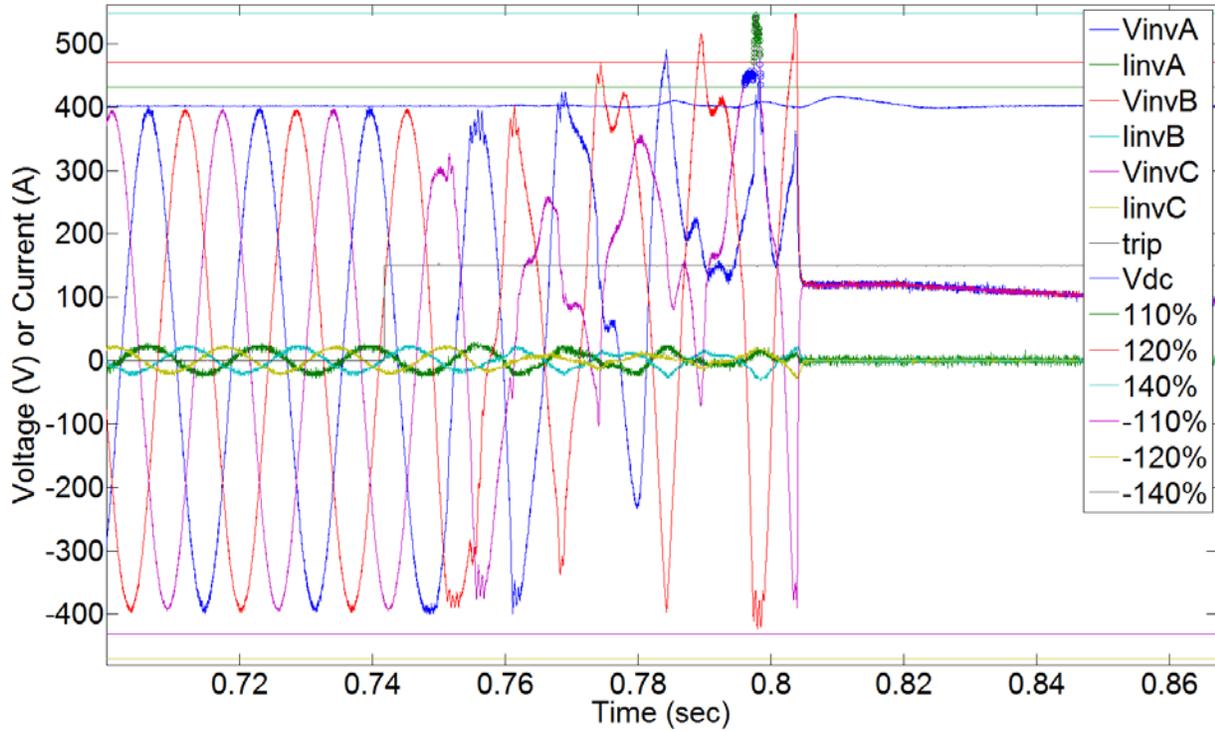


Figure 38: Inverter 4 waveform at unity load ratio - 100% power (P11\_0000)

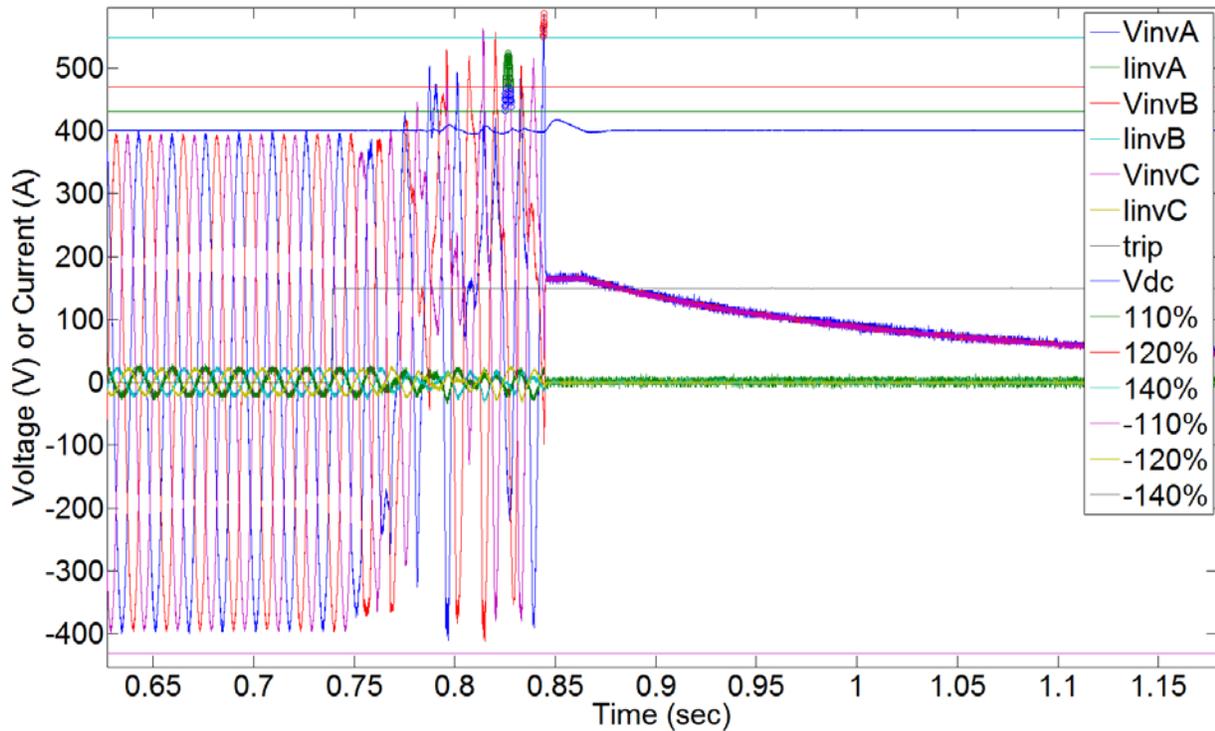


Figure 39: Inverter 4 waveform at unity load ratio - 100% power (P11\_0001)

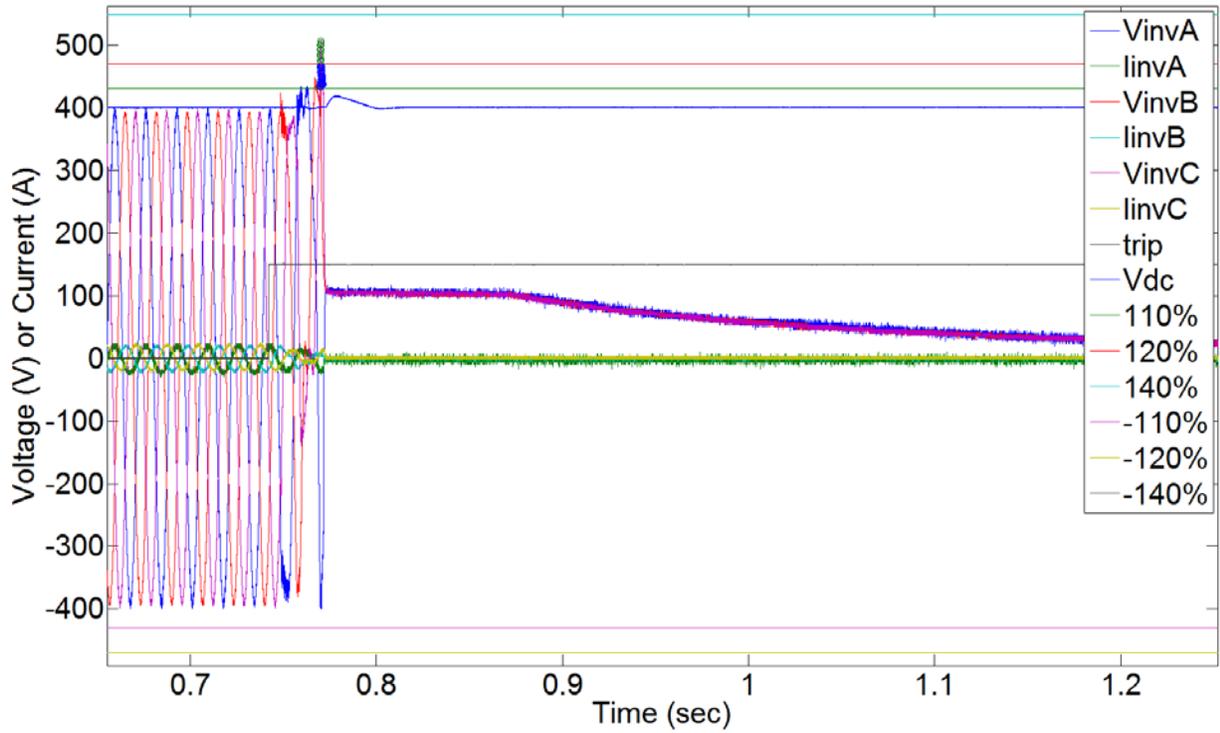


Figure 40: Inverter 4 waveform at medium load ratio – 100% inverter / 67% load power (P61\_0001)

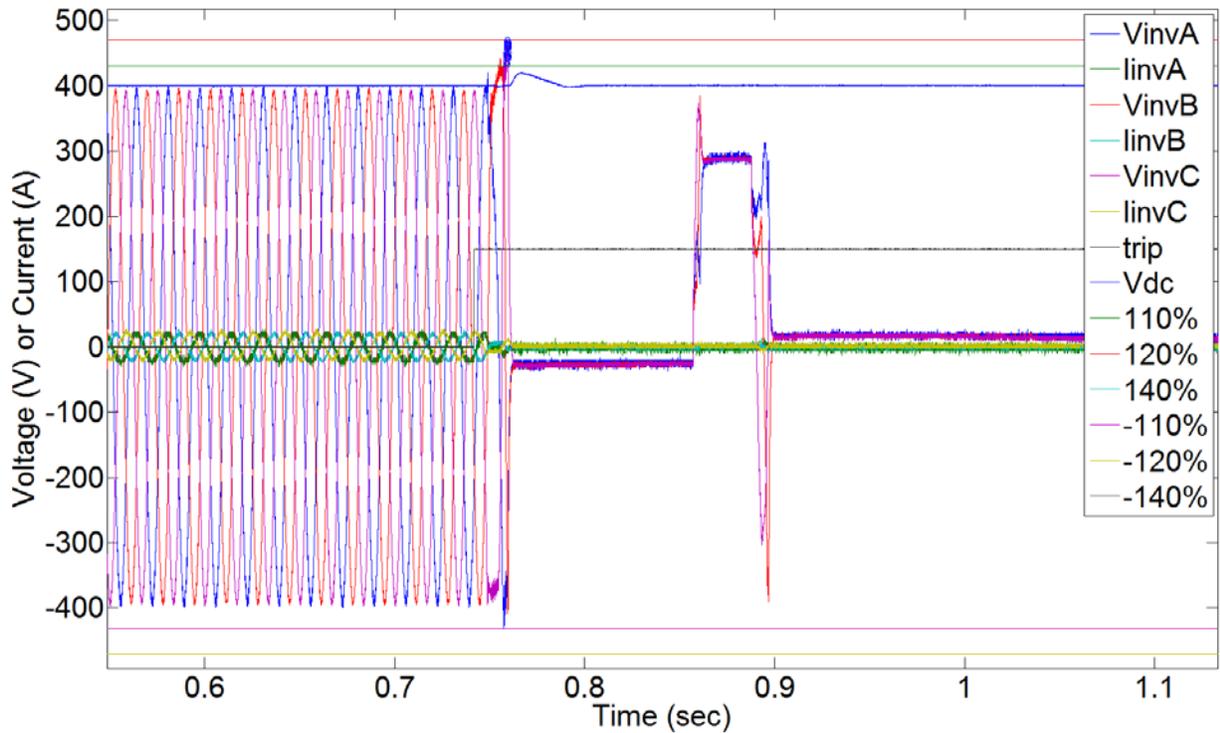


Figure 41: Inverter 4 waveform at medium/high load ratio – 100% inverter / 33% load power (P31\_0005)

### Inverter 5 Waveforms

The response of Inverter 5 was very repeatable, and characterized by one of two waveform types, as seen in Figure 42 and Figure 43. No intermediate or other waveform types were observed. At unity or low load ratios, the inverter output a sinusoidal waveform near the nominal voltage for a couple of AC cycles before quickly disconnecting, as seen in Figure 42. At medium to high load ratios, the inverter would rapidly shut down after one quick over-voltage spike of varying magnitude, as seen in Figure 43. This particular waveform was the worst case over-voltage measured on this inverter, but lasted a very small amount of time. This inverter consistently shut down the quickest after outputting an instantaneous spike in voltage.

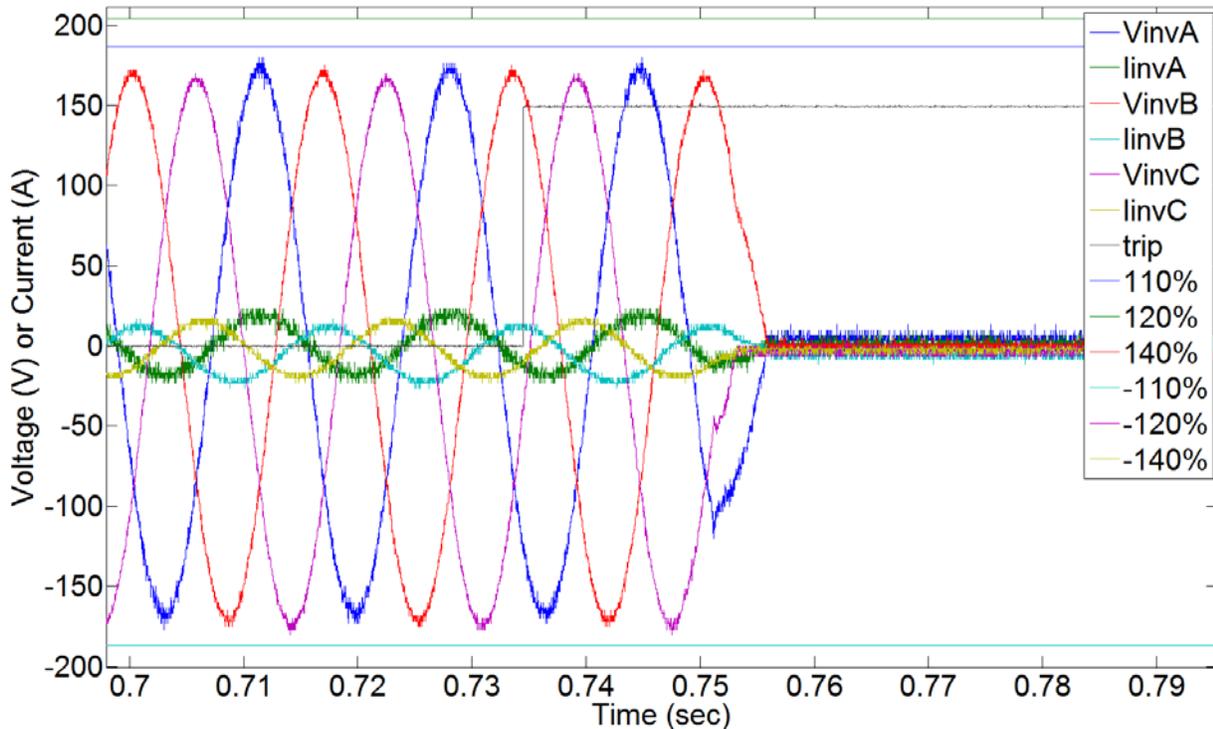


Figure 42: Inverter 5 waveform at unity load ratio – 100% power (N11\_0000)

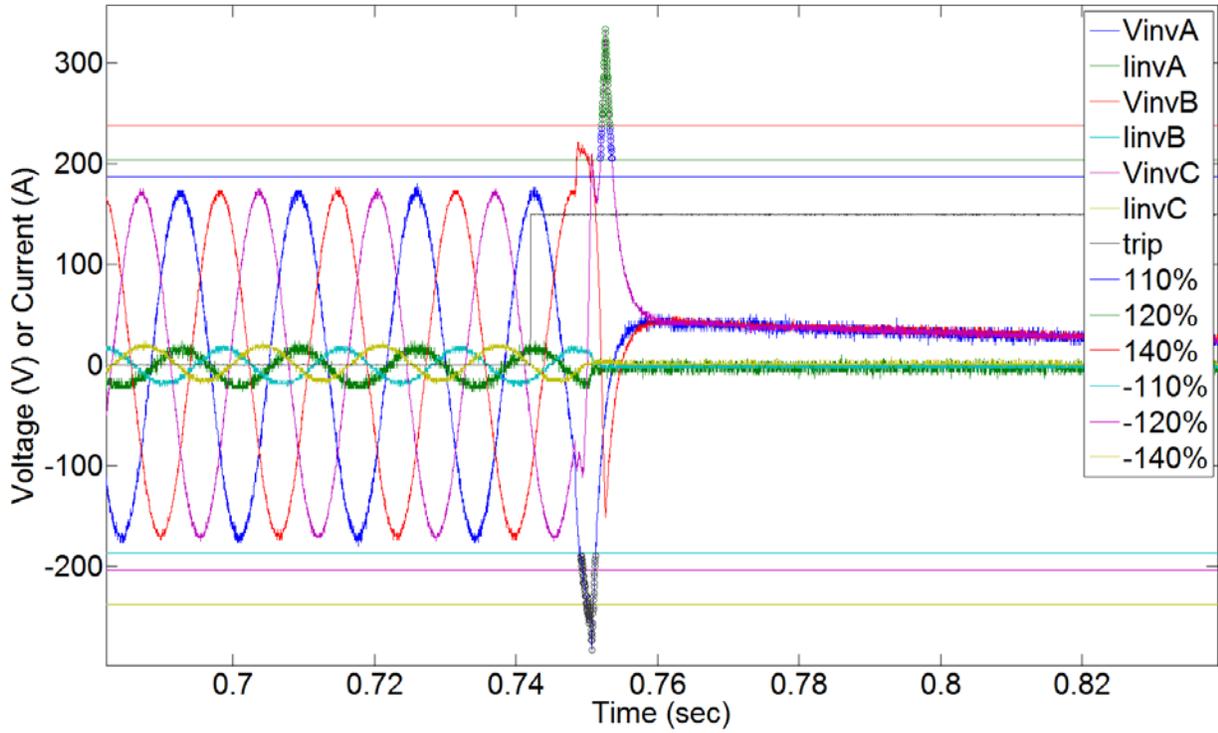


Figure 43: Inverter 5 waveform at high load ratio – 100% inverter / 10% load power (N01\_0003)

### 3.6 Effect of DC Input Voltage on AC Over-voltage

For single-stage inverters, some of the output responses observed in the previous section indicated that the test inverter could meet or exceed the DC input voltage for a significant period of time. An additional short study on the effect of DC input voltage on the magnitude of AC over-voltage was completed to examine this relationship. The additional tests were completed on Inverter 2 and Inverter 4, which are a single-stage, single-phase inverter and a transformerless three-phase inverter, respectively.

A plot of the maximum and average (across five tests) instantaneous AC voltage measurements is shown in Figure 44 for Inverter 2. The inverter was tested five times each at 370 V<sub>DC</sub>, 430 V<sub>DC</sub>, and 490 V<sub>DC</sub>. These tests were performed at 100% inverter power and 10% load power. These tests span most of the inverter MPPT input voltage range, and it is considered a worst case loading scenario. There is possibly a positive correlation between input voltage and maximum output voltage, but it is not clear at higher voltages, and the inverter tended to maintain the higher voltages for a shorter period of time. Figure 45 shows a typical response at the lower end of the input range, where the inverter output an irregular square wave (indicating over-modulation) for a handful of AC cycles. At higher DC input voltages, the inverter tended to trip very quickly after a brief over-voltage, as seen in Figure 46, likely because fast over-voltage or dv/dt trip limits were reached.

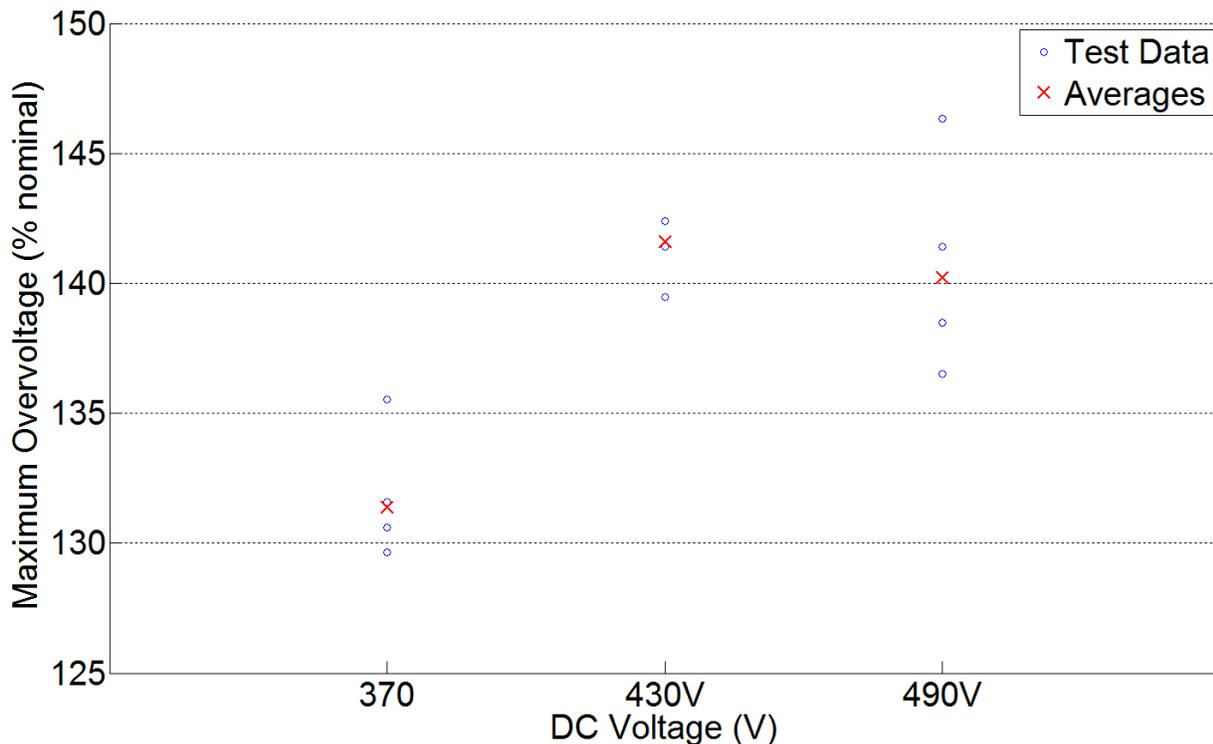


Figure 44: Maximum AC over-voltage as a function of DC input voltage for Inverter 2

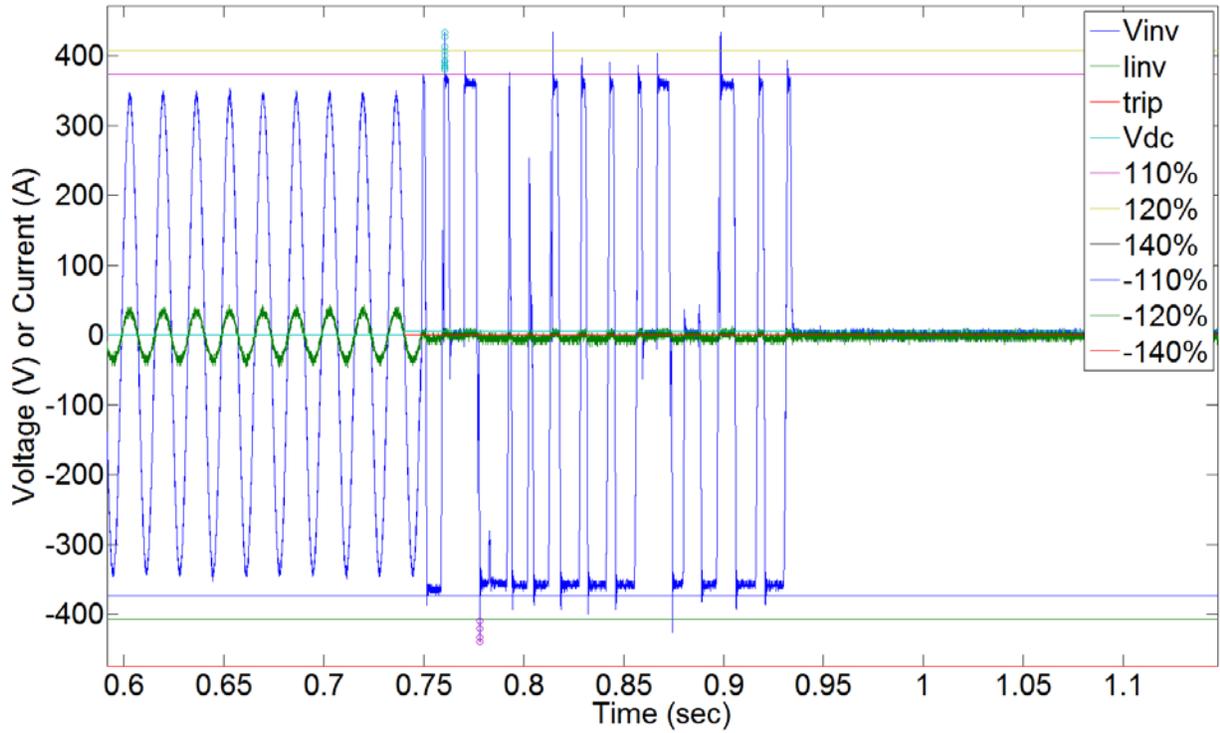


Figure 45: Typical Inverter 2 response for 370 V<sub>DC</sub> input

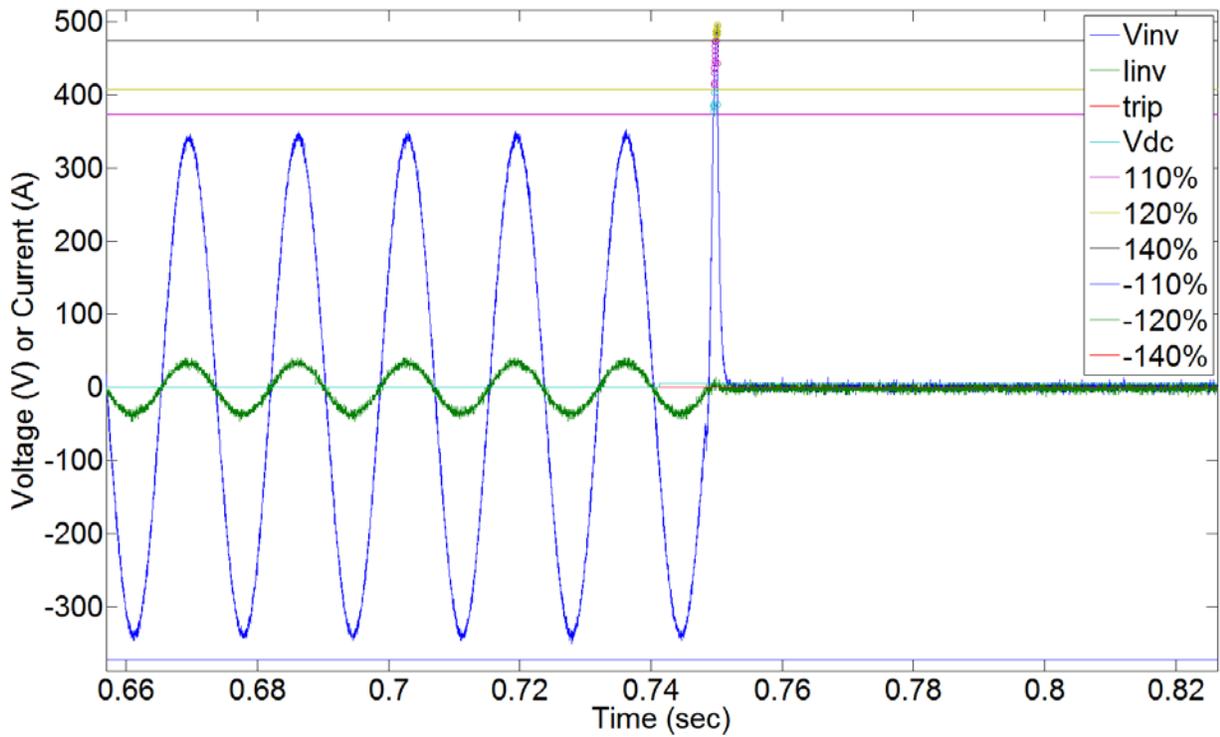
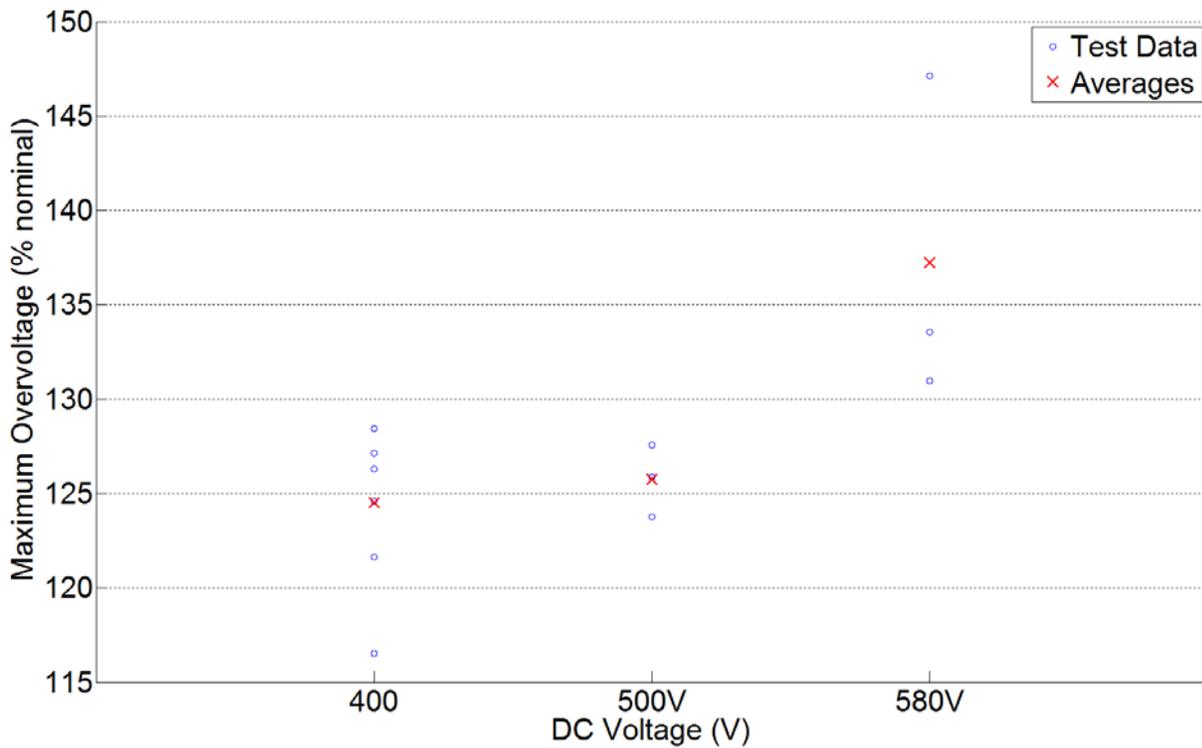


Figure 46: Typical Inverter 2 response for 490 V<sub>DC</sub> input

A plot of the maximum and average instantaneous AC voltage measurement is shown in Figure 47 for Inverter 4. The inverter was tested seven times at 400 V<sub>DC</sub>, and three times each at 500 V<sub>DC</sub> and 580 V<sub>DC</sub> in order to cover the manufacturer’s stated MPPT input range. The inverter was tested at 100% inverter power and 10% load power to test a worst case loading scenario. There is possibly a positive correlation between the input voltage and the maximum output over-voltage, but the magnitude of the over-voltage is relatively low. Typical responses at 400 VDC and 580 VDC are shown in Figure 48 and Figure 49, respectively. In both cases (and also in the intermediate 500 VDC case) the inverter typically tripped quickly after a high instantaneous voltage event. This waveform indicates that the AC terminals can reach the same level as the DC input voltage or a bit higher, but only for a small period of time in these tests.



**Figure 47: Maximum AC over-voltage as a function of DC input voltage for Inverter 4**

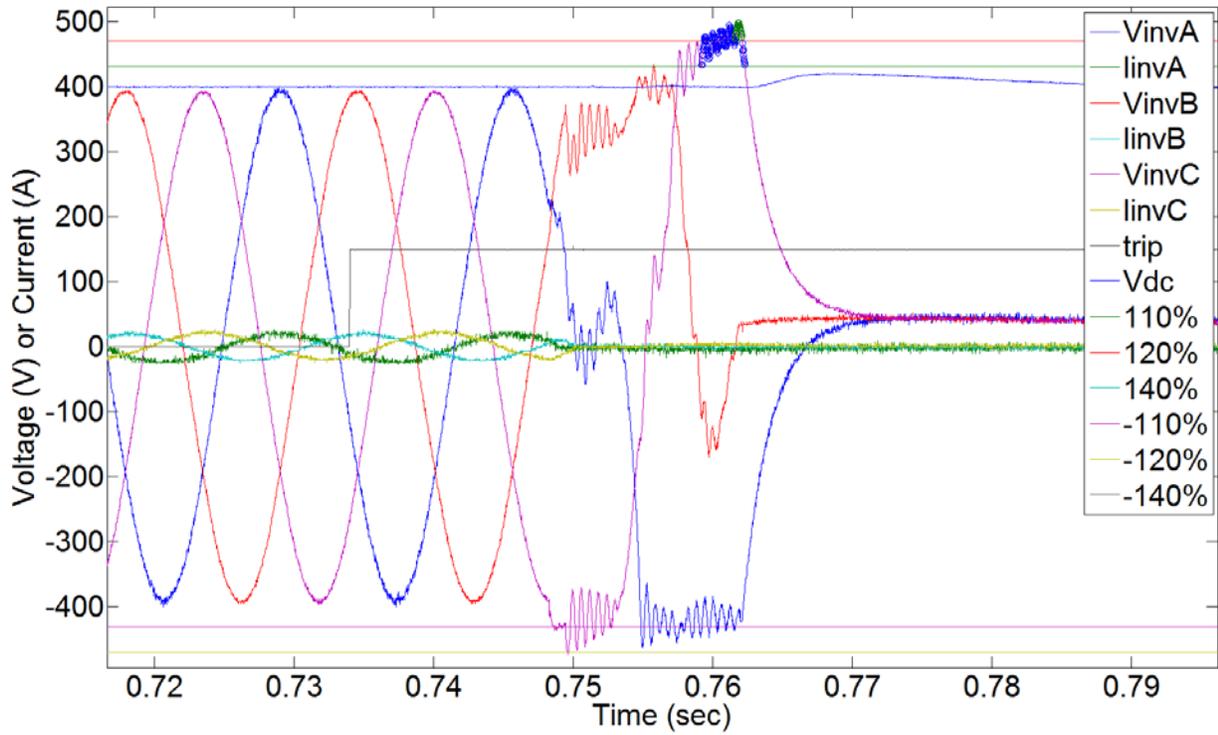


Figure 48: Typical Inverter 4 response for 400 V<sub>DC</sub> input

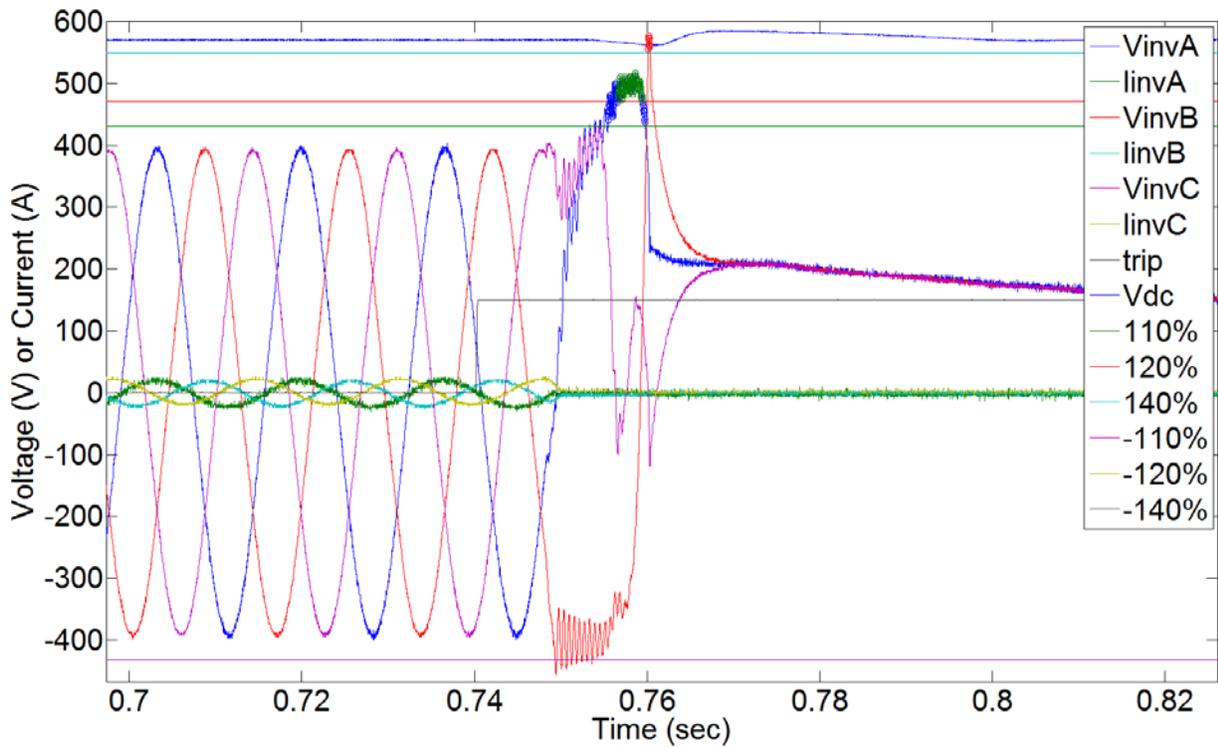


Figure 49: Typical Inverter 4 response for 580 V<sub>DC</sub> input

### 3.7 No-Load Test Results

An additional set of tests was completed on Inverters 2, 3, 4 and 5 to examine the maximum over-voltage measurements when no load was present at the inverter terminals. This set of testing is beyond the scope of the CRADA and the FIGII test plan. Since there is no load, over-voltages observed during these tests do not present a threat to nearby equipment, but instead primarily affect the inverter itself.

A total of seven tests were completed at 100% inverter power and no load, representing an absolute worst case scenario with respect to load rejection over-voltage. A plot of the maximum instantaneous voltage measurement averages and individual test points for each of the four inverters is shown in Figure 50. The largest over-voltage measurement across all tests was 199.2% of nominal and is shown in Figure 51. Most inverters were characterized by a similar behavior where one large over-voltage spike would cause the inverter to quickly shut down. Typically, there would be a long tail on the voltage waveform, due to the natural voltage decay of the inverters' output filter elements without the presence of the load to dissipate the stored energy.

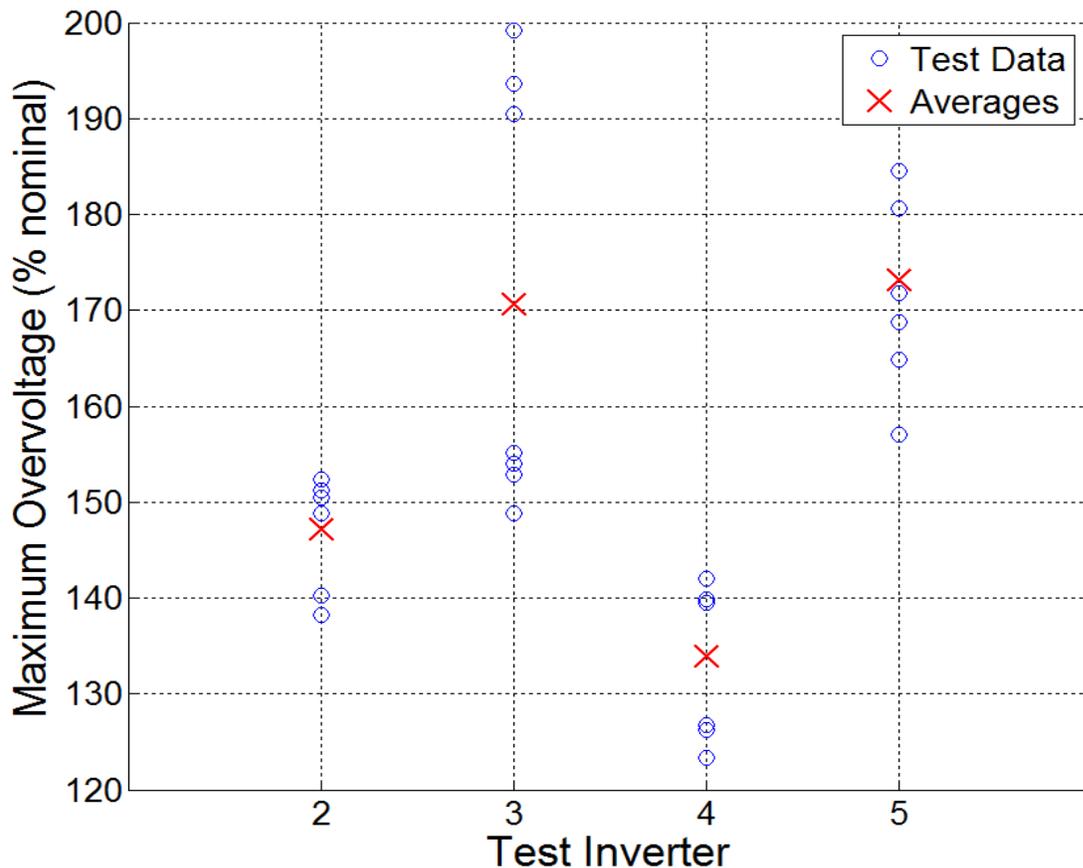
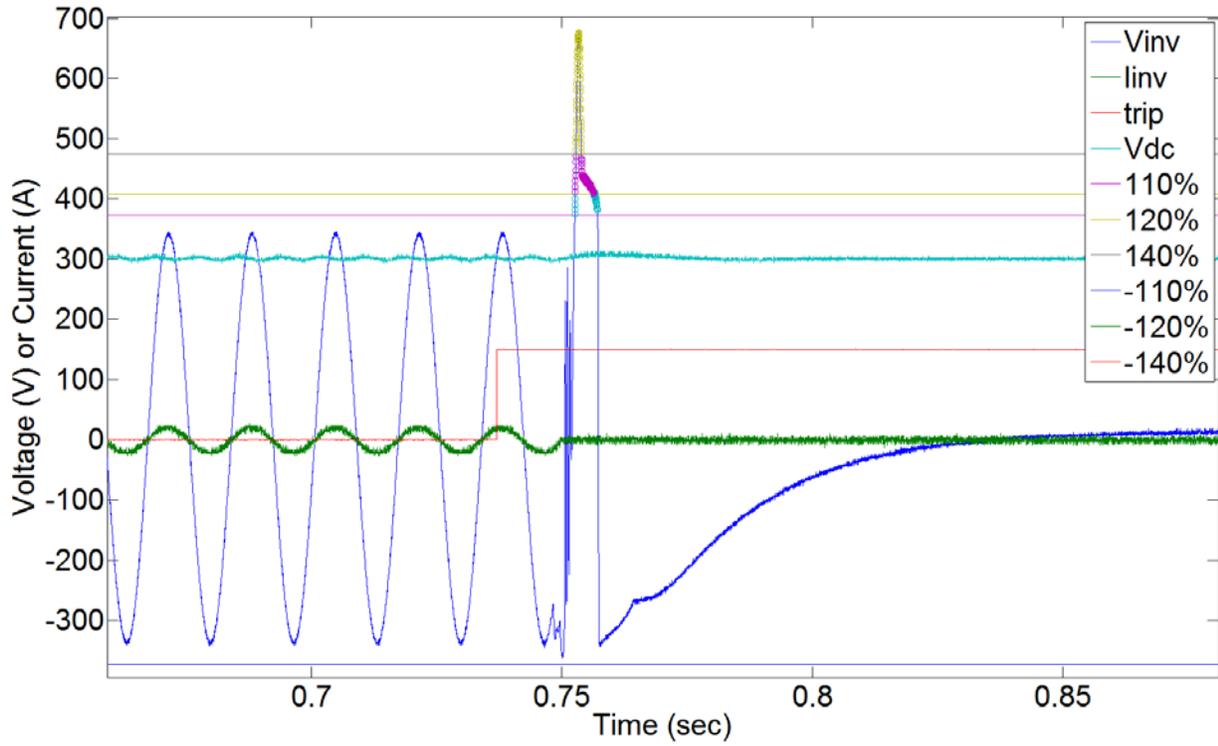


Figure 50: Maximum over-voltage measurements for each of four test inverters at 100% output power, no load



**Figure 51: Inverter 3 waveform at 100% output power, no load**

## 4 Test Procedure Recommendations

Based on lessons learned during LRO testing, the following modifications to the FIGII draft test procedure are recommended for consideration:

- Specify the DC input voltage required for the test procedure. While it is currently unclear if there is a strong correlation between input voltage and output over-voltages, it may be useful to specify that inverters are tested at the minimum, average, and maximum DC input voltages specified by the manufacturer.
- Verify that switch S3 is opened at different parts of the AC cycle. It is unclear if there is a correlation between phase angle at disconnect and the over-voltage duration times, but efforts should be made to randomize the disconnect time.
- As voltage and frequency ride-through capabilities become more common, consider requiring tests at the limits of the ride-through capabilities. It is unclear if the magnitude of over-voltage will be affected, but durations could increase.
- The over-voltage thresholds defined in Table 2 are skewed high based on these test results. Consider eliminating the 500% of nominal threshold and adding a threshold at 170% of nominal, and possibly at other levels.
- As done in this report, record both the *total* time above a given voltage threshold as well as the *maximum continuous* time above a given voltage threshold.
- As done in this report, record the maximum instantaneous voltage measurement recorded at any point during the transient event.
- When possible, disable the 300 second countdown timer for the inverter to start up in order to accelerate testing time. This should not be part of test requirements, but is instead suggested as a best practice.

## 5 Conclusions and Future Work

The load rejection over-voltage test plan implemented at NREL in partnership with SolarCity succeeded in experimentally quantifying load rejection responses of five commercially available grid-interactive inverters. The test plan was based on one developed by FIGII (formerly ITFEG) through a consensus of various stakeholders. The measured over-voltage magnitudes were all under 200% of nominal peak voltage, and the over-voltage durations were on the order of microseconds to milliseconds. These over-voltages were less severe than some observers had feared and have allayed some utility concerns. These results corroborate the theory that in LRO situations, treating inverters as ideal AC current sources greatly overestimates the severity of the over-voltage. The results presented here also show that conducting LRO tests with no load present can lead to an overestimate of over-voltage magnitude.

This report intentionally does not attempt to impose pass-fail criteria on the test results for two reasons: 1. This test plan is not yet standardized; a much simpler test may be possible, as mentioned below. 2. Any pass-fail criteria should be developed through a consensus-based process including various industry stakeholders and taking into account the best available information on distribution system requirements.

Future work on this topic should include development of detailed inverters models that can be used to simulate LRO scenarios of interest to utilities, inverter manufacturers, PV project developers, electricity end-users, and other stakeholders. The data presented in this report can be used to develop and validate those models.

Due to the limited number of inverters tested, future work should also expand the range of inverter sizes and topologies tested, as well as additional testing of similar inverters to obtain a more representative sample. This is especially true for three-phase inverters as only one model was tested here. Inverter load rejection responses vary between inverters, as clearly illustrated by the single-phase inverter results presented here.

In addition, it would be reasonable to include some type of LRO test into standardized certification tests that inverters typically undergo. While a detailed test such as the one used here could serve that purpose, it may also be worth considering a test that simply ensures that inverters cease to energize the grid within some very short time of the appearance of a high over-voltage (i.e. a test similar to over-voltage tests currently used in IEEE Standard 1547.1 and UL 1741 but with a higher disconnection magnitude and shorter duration).

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